FR-10119

Final Technical Report For:

MOCVD PROCESS TECHNOLOGY FOR AFFORDABLE, HIGH-YIELD, HIGH-PERFORMANCE MESFET STRUCTURES

MIMIC PHASE 3

Submitted Under:
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Submitted To:
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Washington, D.C.

spire

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St-A per telecon Mr. Marshall, Naval Air Sys Comd/ADPO-48. Wash., DC 20361-9330.

3-1-93 JK

LIST OF ILLUSTRATIONS

SECTION 1
INTRODUCTION

Under the MIMIC Program, Spire has pursued improvements in the manufacturing of low cost, high quality gallium arsenide MOCVD wafers for advanced MIMIC FET applications. As a demonstration of such improvements, Spire was tasked to supply MOCVD wafers for comparison to MBE wafers in the fabrication of millimeter and microwave integrated circuits. In this, the final technical report for Spire's two-year MIMIC contract, we report the results of our work.

1.1 PROGRAM OBJECTIVES

The main objectives of Spire's MIMIC Phase 3 Program, as outlined in the Statement of Work, were as follows:

- Optimize the MOCVD growth conditions for the best possible electrical and morphological gallium arsenide. Optimization should include substrate and source qualification as well as determination of the optimum reactor growth conditions.

- Perform all work on 75 millimeter (3") diameter wafers, using a reactor capable of at least three wafers per run.

- Evaluate epitaxial layers using electrical, optical, and morphological tests to obtain thickness, carrier concentration, and mobility data across wafers.

- The thickness of the layers shall vary by no more than ±3 percent over 80 percent of a wafer, while doping shall vary by no more than ±5 percent over 80 percent of a wafer. These uniformities shall be maintained within a wafer, among wafers in a run, and among batches of wafers.

- Undoped layers should have good photoluminescence as well as impurity concentrations below 1×10^{15} cm^{-3}. The room temperature mobility shall be no less than 7,500 $cm^2V^{-1}s^{-1}$.

The Statement of Work listed several tasks in support of the objectives. Among these were modification of the MOCVD apparatus, characterization of substrates prior to use, establishment of procedures and optimum conditions for epitaxial growth in the modified reactor, and characterization of the epitaxial layers.

Once having established the capability to grow high quality epitaxial layers on 75 millimeter wafers, Spire was to supply no fewer than 50 MESFET wafers to a MIMIC Phase I contractor for insertion into the fabrication line and comparison to MBE material. The MIMIC Phase I contractor was to inspect and qualify the wafers, and provide material and device performance to allow further optimization of the epitaxial growth procedures. The Phase I contractor was also to provide yield information for all process steps so that Spire could develop a cost model comparing MOCVD to MBE for MIMIC MESFET integrated circuits.

SECTION 2
PROGRAM PROGRESS

2.1 SUMMARY OF PROGRESS

The most significant progress during the program was the completion of all major modifications to the MOCVD apparatus and the demonstration of epilayer uniformity exceeding the program goals of ±3 percent in thickness and ±5 percent in doping, on 75 millimeter diameter substrates.

We also completed a series of experiments to qualify substrates and identify substrate preparation techniques, and completed a cost model showing that MOCVD MESFET wafers can be produced for as little as $700 or less using the modified reactor.

Spire produced eight FET wafers for delivery to the Phase I contractor. The wafers exhibited Polaron doping profiles that raised concerns about possible buffer leakage. Spire worked to grow acceptable wafers by modifying the reactor growth conditions. Since the unusual doping profiles may have resulted from shortcomings in the C-V measurement technique, Spire asked the contractor to evaluate the wafers fully by fabricating and testing finished FET devices on them. This technical issue was not resolved in time to deliver the remaining wafers specified in the Statement of Work.

Figure 2-1, a milestone chart, shows the progress against the major tasks for the first year of the program. As shown in the chart, we grew 26 of the required 50 wafers and delivered 18. Some device fabrication and related tasks were not completed because of the technical questions concerning the eight FET wafers.

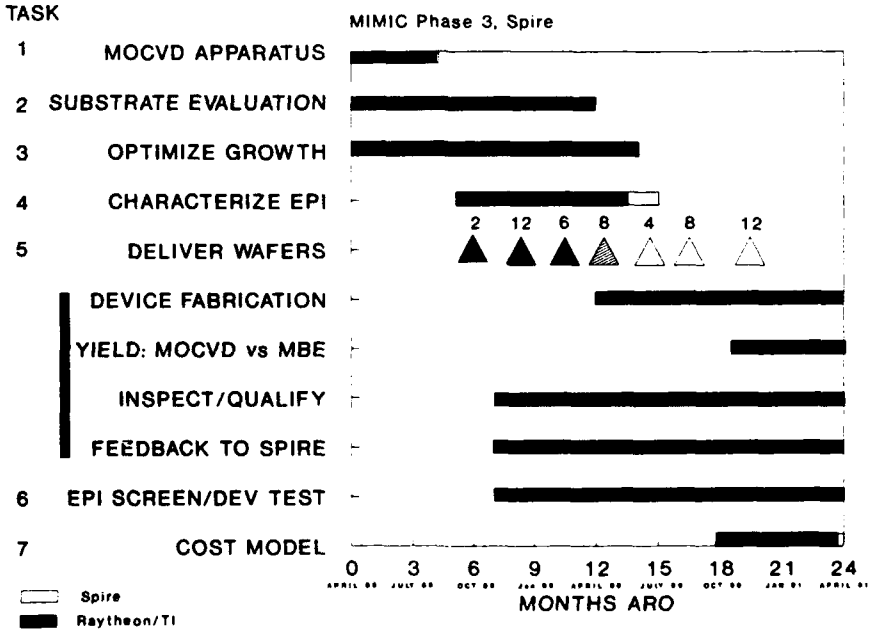


FIGURE 2-1. TASKS AND MILESTONES CHART.

spire

26 January 1993

Defense Technical Information Center
Cameron Station, Building 5
Alexandria, VA 22304-6145

Attn: Selections

Subj: FINAL REPORT UNDER CONTRACT No. N00019-89-C-0152

Ref: 4200 Ser AIR-21633N/93-004

Dear Sir/Madam:

In reponse to the letter of the above referenced number, I am enclosing a reproducible copy of our final report submitted 28 January 1991, including the letter of transmittal.

If you have any further questions please contact Mr. Michael O'Dougherty, Manager, Contracts.

Yours truly,

SPIRE CORPORATION

Pauline M. Cooke

Pauline M. Cooke
Coordinator, Publications

Enclosure

Spire continues to work on understanding FET doping profiles and controlling buffer leakage. Since completion of the program, we have supplied 75 millimeter diameter FET wafers to several firms for qualification. We expect that Spire's MOCVD-grown FET wafers will still prove to be a viable alternative to MBE wafers for the MIMIC program and for commercial applications

2.2 TASK 3.1 - MOCVD APPARATUS

Figure 2-2 presents a schematic illustration of the reaction chamber to the SPI-MO CVD™ 1200 system, a new, large-scale MOCVD reactor that we modified for producing high quality MESFET material for this program. The reactor can deposit crystalline layers on fourteen 50 millimeter diameter or seven 75 millimeter diameter wafers simultaneously. The gas flow dynamics of the reactor have been investigated theoretically by computer modelling and experimentally by flow visualization ("smoke") tests. The reaction chamber features a hollow, barrel-type, silicon carbide-coated graphite susceptor with seven facets tilted ten degrees from the vertical. Each facet has recesses to accommodate two 50 millimeter wafers or a single 75 millimeter wafer.

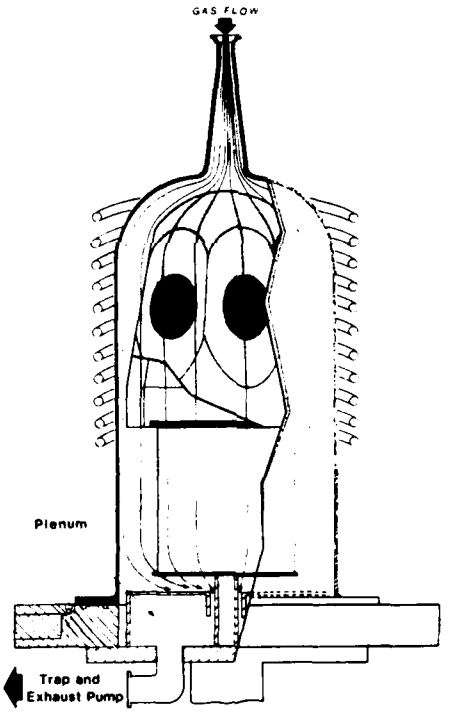


FIGURE 2-2. SCHEMATIC ILLUSTRATION OF THE SPI-MO CVD™ 1200 REACTION CHAMBER.

During the first year of this program, we used a susceptor holding six 75 mm and two 50 mm wafers. The quartz bell jar has a 25-centimeter inner diameter, is approximately 70 centimeters tall, and is shaped to follow the contours of the susceptor. An external RF coil heats the susceptor inductively to a preset temperature which is monitored by an optical pyrometer that views the inside of the susceptor through a sapphire light pipe. The gas delivery system is of standard commercial design and has been described previously.[1]

2.2.1 Summary of Previous Research

Prior to the MIMIC program, Spire conducted research to further the development of large-area deposition for producing high efficiency solar cells.[1] This earlier work suggested that, with the appropriate modifications, the model MO CVD 1200 reactor could produce high quality, low cost MESFET material.

The steady-state operating conditions of the reactor were modelled using a numerical technique described previously.[2,3] The model simultaneously solves the equations of continuity, motion, differential thermal energy balance, and mass conservation for the various species in an axi-symmetric system. Allowance was made for variable property (temperature and composition dependent) values. The predicted flow pattern for operation at 0.1 atmospheres and 40 standard liters per minute (slpm) total gas flow rate is shown in Figure 2-3 along with the experimentally observed flow pattern obtained by titanium dioxide smoke tests.

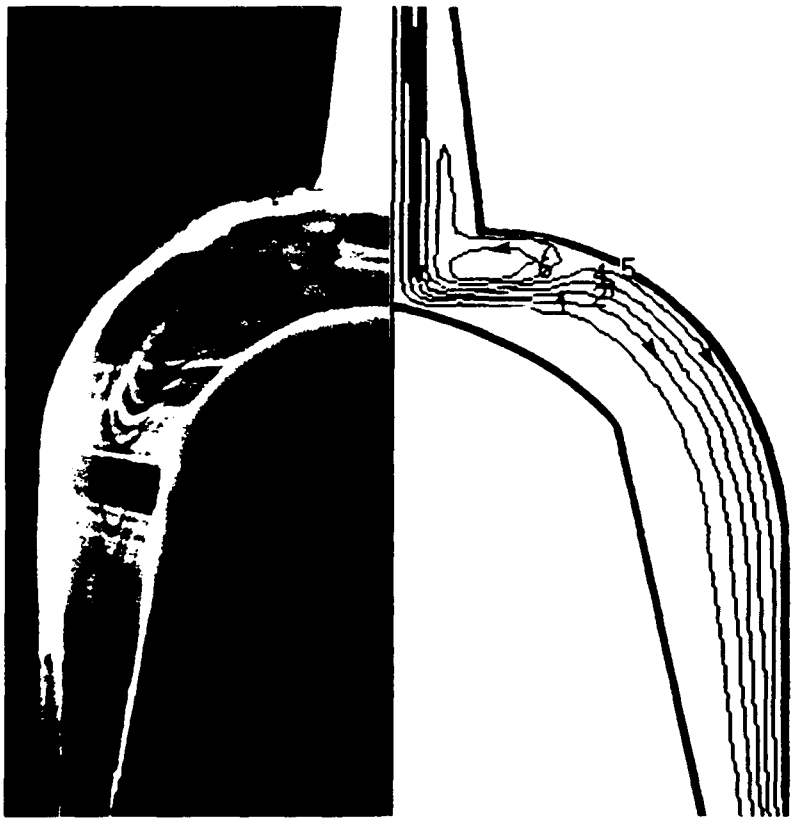


FIGURE 2-3. COMPARISON OF THEORETICAL (RIGHT) AND EXPERIMENTAL (LEFT) FLOW PATTERNS.

As seen in the figure, at low pressure, gas flow in this reactor exhibits a streamlined laminar flow pattern. This implies that reactor pressure, gas flow rate, and susceptor tilt control uniformity, as in many horizontal flow reactors. With the suppression of recirculation loops observed during laminar flow, the gases in the reactor can be flushed out very quickly, which will allow the growth of abrupt hetero-interfaces.

The computer modelling and flow tests demonstrated that keeping the interior of the reaction chamber as uniform as possible in temperature helps to suppress convection currents and maintain laminar flow conditions. Therefore, it is desirable to disable the water cooling of the reaction chamber bell jar so that the interior surfaces do not cool and disrupt the gas flow. However, this subjects many parts of the reactor to higher operating temperatures and requires the exhaust system to handle reaction by-products that previously deposited on the bell jar under cold wall conditions. For the MIMIC program, Spire proposed modifications to the reactor for warm wall operation, followed by characterization and optimization of the operating conditions for MESFET growth.

2.2.2 Modifications to the Apparatus for MIMIC

Spire designed and installed a bell jar capable of withstanding, without water cooling, the 500 to 1100°C temperatures needed for MOCVD growth. The bell jar features a flow disrupter of proprietary design to distribute the incoming gases evenly across the wafers mounted on the susceptor.

As expected, the first operational tests led to exhaust clogging from arsenic and gallium deposits. To overcome this problem, we added a large central exhaust port to the bell jar base plate and sealed the small exhaust holes that had previously clogged. To limit the amount of arsenic and gallium reaching the pump, we installed a cold trap in the exhaust line, below the bell jar. This not only reduced corrosion of the vacuum pump, but also made cleaning the exhaust line easier.

Other modifications were required for operation at the higher temperatures and flow rates needed for warm wall operation. Spire installed new higher capacity mass flow controllers, bubbler control valves, and gas flow lines, and then modified the "pump & purge" and "pause" computer routines for reactor operation at high flows. We also installed additional dilution lines for silane and disilane dopant gases. We designed, fabricated and installed a new base plate to bell jar sealing mechanism using heat resistant Viton "O-rings". We constructed a new rf inductive heating coil designed to allow adjustment of winding spacing for control of susceptor heating uniformity. The coil features supports made from a heat resistant silica fiber composite ceramic. Spire also fabricated a heat resistant pyrometer light pipe employing Viton seals. Other modifications included rf shielding, plumbing, cooling, and safety interlock changes to reduce maintenance and provide safety to the operators.

During the first operational tests we attained susceptor temperatures in excess of 1100°C, and reaction chamber flow rates of up to 60 slpm. We then conducted growth tests with 75 millimeter diameter substrates. All tests were conducted using arsine and trimethylgallium diluted with hydrogen to supply the gallium and arsenic for epitaxial growth. We maintained the

chamber pressure at approximately 70 torr, just above the pressure at which rf induction causes electrical break down of the gases and formation of a plasma.

With a flow rate of 60 slpm, we attained an epitaxial layer thickness uniformity of ±5 percent. To improve the uniformity, we needed higher flow rates, therefore we installed two 50 liter/minute mass flow controllers and added a second vacuum pump in parallel with the first. In subsequent experiments, we attained flows of up to 100 slpm and verified that the optimum flow rate for thickness uniformity was between 50 and 90 slpm.

After the exhaust gases leave the vacuum pumps, we burn them and pass the combustion products through an HEPA filter on the roof of the building. During the high flow rate experiments, the heat produced by the combustion of the exhaust gas caused the HEPA filter to start to decompose. To solve this unanticipated problem, we acquired and installed high temperature filters.

2.2.3 Additional Modifications For High Quality Material

After the first operational tests of the reactor, Spire installed a new high purity, high flow rate hydrogen gas system for the reactor. We had placed an order for the system, to be paid for outside of the MIMIC program, in the early spring of 1989. This system is needed to ensure epitaxial material with low levels of background impurities and good doping uniformity.

The heart of the system, a three-stage metal hydride pump, requires a high capacity water heater to drive the hydride reaction and produce the pressurized hydrogen needed to maintain flow through the hydrogen purifier. The water heater and booster pump required:

- High capacity hydrogen supply lines and output lines to the MOCVD reactor, including pressure regulators and valves,
- Large diameter natural gas supply line for the water heater, as well as combustion air and exhaust ducting isolated from the class 100 environment of the laboratory,
- Electrical supply and control wiring.

Spire completed the extensive work needed to install and test the hydrogen booster pump and purifier in early December, and with all the major modifications to the apparatus completed, we next concentrated on finding the optimum growth conditions for high quality epitaxial material.

2.3 TASK 3.2 - CHARACTERIZATION OF SUBSTRATES PRIOR TO USE

Because of the variability of vendors' substrates, Spire routinely samples substrates from all substrate vendors. Only wafers of the highest quality are accepted.

During the first year of Spire's MIMIC program, we inspected incoming substrates for dimensional tolerances, front and back surface quality, orientation, crystallographic quality

including etch pit density and distribution, and electrical parameters. All wafers were subjected to front surface and back surface inspection visually under oblique illumination, and, in some cases, at a magnification of 32 under a Wild 420 Macroscope. When possible, Spire selected three wafers from each boule, with position origin in seed end, middle, and tail end, for destructive evaluation, including electrical characterization, thermal stability testing, and etching to reveal subsurface damage and etch pit density. Substrates that passed our characterization tests included lots from Airtron, American Crystal Technology (AXT), Hitachi, M/A-COM, Semitronic, Spectrum Technology, Sumitomo, and Wacker.

2.4 TASK 3.3 - OPTIMIZE PROCEDURES FOR EPITAXIAL GROWTH ON SUBSTRATES

This task consists primarily of two subtasks, determining the best technique for selecting and preparing the substrates prior to epitaxial growth, and the determining the optimum reactor growth conditions for high quality material for MESFETs.

2.4.1 Substrate Preparation

In spite of Spire's rigid quality control inspection of incoming substrates, many produce poor MESFETs by MOCVD, primarily because of high buffer leakage currents. This buffer leakage problem occurs with certain vendors' substrates at any one time, but may occur with substrates from other vendors at other times. For the MIMIC program, Spire embarked on a series of experiments designed to provide additional criteria for screening substrates, as well as preparation techniques that might allow the use of otherwise unacceptable substrates.

In summary, the experiments showed that:

- The only vendor that provided substrates that consistently gave us low buffer leakage was Hitachi.
- Wacker and Airtron substrates also gave us good results, but not consistently.
- Spectrum's specially polished "Spectrum-B" substrate, subjected to an arsine bake out, gave excellent results, but we were not able to repeat the test on additional substrates because Spectrum went out of business.
- The bake out treatment was not effective with substrates from other vendors.
- A light etching followed by a mechanical scrubbing of the substrate appeared effective in removing surface contamination. If the substrate surface showed no evidence of contamination, this treatment caused slight worsening of the buffer leakage.
- Auger electron spectroscopy tests failed to identify the source of surface contamination on the suspect substrates.

Prior to the start of Spire's MIMIC program, Spire and Alpha Industries conducted joint research into MOCVD MESFET fabrication. As outlined in Spire's April 1989 Monthly Progress Report, this research suggested that buffer leakage frequently results from substrate surface contamination. We speculated that this contamination could result from improper post-polish cleaning, oxides from exposure to the air, or organic compounds such as plasticizers from improper storage. The elimination of surface contamination was one of the major goals of our substrate experiments.

2.4.1.1 Experiment One - Vendor Test

Spire contacted Spectrum Technology to discuss surface contamination, and Spectrum supplied wafers cleaned by two different proprietary post-polish methods for evaluation. We also received substrates from Wacker, Airtron, and Hitachi which the vendors represented as suitable for MOCVD MESFET growth. We subjected all of the substrates to our quality control inspection, as detailed in Section 2.2. Only those deemed acceptable were used for the substrate experiment.

To evaluate the substrates, Spire employed the same in-house procedure used during the joint effort with Alpha:

1. The structure shown in Figure 2-4 is grown during one run in the MOCVD reactor:

   1) SI GaAs substrate
   2) 1.0 μm undoped GaAs buffer layer
   3) 0.16 μm GaAs N=5E17 cm^{-3} active layer
   4) 0.10 μm GaAs N = low E18 cm^{-3} cap

2. After growth and removal from the MOCVD reactor, a layer of Au/Ge ohmic contact metal is deposited on the surface of each wafer.

3. The contact, cap, and active layers on each wafer are masked and chemically etched away, exposing the buffer layer between mesas topped with contact pads (see Figure 2-5).

4. Leakage current is measured against applied voltage for adjacent pairs of pads across each wafer. A good wafer should have a buffer resistance as determined from the IV curve of at least three megohms per square. Under background room lighting conditions, these wafers will exhibit leakage of only a few microamperes with an applied voltage of 10 volts. The acceptance criterion for buffer leakage is a buffer resistance of better than 2 megohm per square.

Table 2-1 shows the mean buffer resistance for seven different substrates processed through to FET test structures. The results in the table show that the Hitachi substrate produced better FETs than did the Airtron or Wacker substrates. However, note the large standard deviation

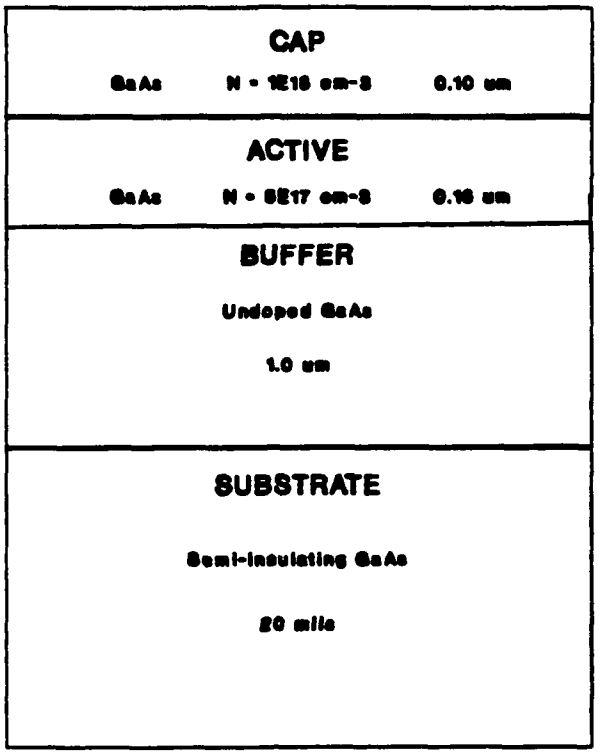


FIGURE 2-4. EPITAXIAL STRUCTURE FOR BUFFER LEAKAGE TESTS.

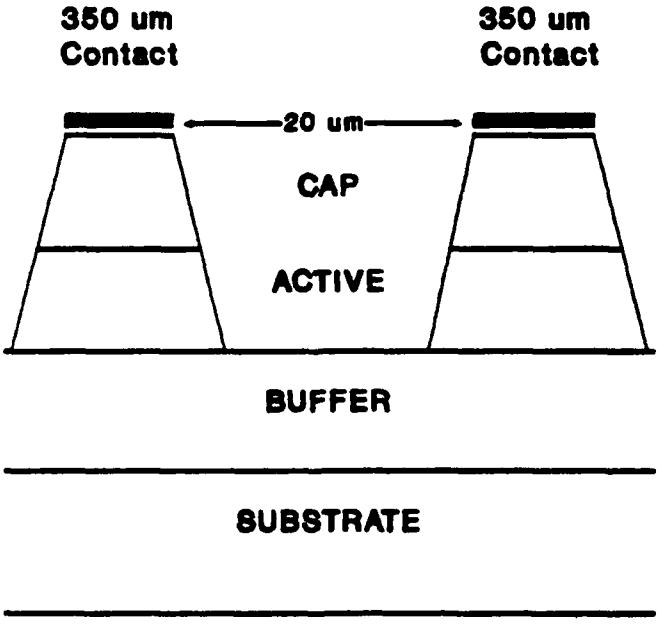


FIGURE 2-5. METAL CONTACT GEOMETRY FOR BUFFER RESISTANCE MEASUREMENTS.

TABLE 2-1. BUFFER LEAKAGE EXPERIMENT #1.

Buffer Resistance By Sample

MOCVD Run No.	Mean Resistance Vendor	Std. Dev. MegOhm/Sq.	MegOhm/Sq.	Number Of Measurements
871-1	Wacker	0.0033	0.0007	6
871-2	Airtron	0.123	0.283	9
871-3	Wacker	0.011	0.0058	8
873-A	Spectrum-A	0.0097	0.0076	6
873-B	Spectrum-B	0.0154	0.0169	6
873-C	Spectrum-C	76.10	62.2	5
881-1	Hitachi	198.	111.	3

for the Hitachi measurements. In paired comparisons using the *student's t-test*, there is a 9.1 percent probability that the differences between the Hitachi and Wacker results are due to measurement scatter alone. Similarly, there is a 9.1 percent probability that the differences between the Hitachi and Airtron results are due to chance.

Spectrum supplied two substrates cleaned by special proprietary techniques. The first, labelled "Spectrum-A", had been subjected to a UV-ozone cleaning treatment. Spectrum cleaned the second substrate, "Spectrum-B", using an experimental polishing technique. We included the "Spectrum-C" substrate, an ordinary, untreated Spectrum substrate, as a control. The untreated "Spectrum-C" substrate produced better buffer resistance than either of the specially treated substrates at a 5.2 percent level of significance.

Statistical testing of the data for all other pairs of vendors did not show the differences in buffer resistance to be significant, because of small sample size and scatter in the data.

Because we used only a single wafer from each vendor, we could not conclude with confidence that all Hitachi or that all untreated Spectrum substrates will produce superior FETs. However, the results suggested that additional experiments with these substrates would be worthwhile.

2.4.1.2 Experiment Two - Bake Test

Scientists at Spectrum Technology told us that heating their treated substrates ("Spectrum-A" and "Spectrum-B") in an arsine over pressure prior to epitaxial growth should

result in better FETs. We speculated that this procedure would remove residual organic surface contamination, if any, from the substrates. We heated slices of the Spectrum A, B, and C substrates in arsine at 720°C for 15 minutes, and then grew and fabricated the FET test structure on them. Table 2-2 shows the results of the buffers' resistance measurements on these and the unbaked samples.

TABLE 2-2. BUFFER LEAKAGE EXPERIMENT #2. Spectrum technology bake out tests.

	Buffer Resistance By Sample				
	MOCVD Run No.	Vendor	Mean Resistance MegOhm/Sq.	Std. Dev. MegOhm/Sq.	Number Of Measurements
	NOT BAKED:				
	873-A	Spectrum-A	0.0097	0.0076	6
	873-B	Spectrum-B	0.0154	0.0169	6
	873-C	Spectrum-C	76.10	62.2	5
Mean:			22.4	47.4	
	BAKED:				
	975-A	Spectrum-A	30.3	30.2	5
	975-B	Spectrum-B	291.	393.	4
	975-C	Spectrum-C	241.	227.	4
Mean:			175.	258.	

As shown in the table, baking a Spectrum substrate improved the buffer resistance in the test devices, whether we started with a treated or untreated Spectrum substrate. However, for the untreated substrate, "Spectrum-C", the baking procedure caused degradation of the surface quality of this wafer to the point where we judged it unacceptable for device fabrication.

Overall, the baked substrates produced better buffer resistance than the unbaked substrates at a 5.5 percent level of significance.

2.4.1.3 Experiment Three - Continuation of Bake Tests

Based on the encouraging results from the bake procedure applied to Spectrum substrates, we decided to test the procedure on substrates from other vendors.

Table 2-3 shows the results of the bake procedure applied to stock substrates, as supplied, with no special treatment, from Spectrum, Airtron, Wacker, and M/A-COM. We also tested a new "super clean" variety of Sumitomo substrate.

On the average, the baking procedure did not improve the buffer resistance. The procedure had no significant effect on the Spectrum sample, while it made the buffer resistance on the M/A-COM wafer much worse. The results for Wacker and Sumitomo were inconclusive because of insufficient data and variations in the fabrication of the test devices.

Comparing the results by vendor, we found that the Wacker substrate produced higher buffer resistance than Spectrum (2.4 percent level of significance), and higher buffer resistance than Sumitomo (2.0 percent level of significance). The Spectrum substrate in turn resulted in higher buffer resistance than Sumitomo (1.4 percent level of significance). Airtron also surpassed Sumitomo in buffer resistance (2.0 percent level of significance). Other comparisons, for example between Wacker and Airtron, showed that the differences between mean buffer resistance were not statistically significant at the 5 percent level.

Once again, we caution against drawing conclusions about overall vendor quality or suitability for epitaxial FETs. Because we used only a single wafer from each vendor, we could not conclude with confidence that the results would be reproduced using a large random sample of the vendors' wafers. Nevertheless, after reviewing the results in Table 2-3, we decided to place an order for Airtron substrates to be used for the first wafer deliveries under the MIMIC program. Spectrum had been our first choice, but these substrates were no longer available by the end of 1989.

TABLE 2-3. BUFFER LEAKAGE EXPERIMENT #3. Continuation of bake out tests.

Buffer Resistance By Sample				
MOCVD Run No.	Mean Resistance Vendor	Std. Dev. MegOhm/Sq.	MegOhm/Sq.	Number Of Measurements
NOT BAKED:				
1160-1	Spectrum	68.0	27.2	4
1160-2	Airtron	70.5	70.0	2
1160-3	Sumitomo	1.80	0.000	2
1160-4	Wacker	0.0029	-	1
1160-5	M/A-COM	71.5	41.1	4
Mean:		63.7	40.6	
BAKED:				
1162-2	Spectrum	63.0	22.0	4
1162-3	Airtron	150.5	65.8	4
1162-4	Sumitomo	32.5	19.8	4
1162-1	Wacker	63.3.	14.8	4
1162-5	M/A-COM	7.90	6.84	4
Mean:		77.3	56.2	

2.4.1.4 Auger Electron Spectroscopy Tests

To test for a correlation between substrate surface contamination and buffer leakage, we subjected FET wafers grown on substrates from Sumitomo, Wacker, and Spectrum to Auger electron spectroscopy (AES). The AES technique produces a spectrum of electron energies from the top 10 to 30Å of material bombarded with 1 to 5 keV electrons. This spectrum can be used to identify the atomic species present. The technique is especially useful for signalling the presence of organic materials such as those that may result from substrate cleaning. We used the Auger technique combined with a sputter etch to allow profiling into the depth of the samples.

We submitted six FET samples for AES profiling through the buffer layers and into the substrates. Small levels of carbon, oxygen, and sulfur were detected on the surfaces of the wafers, diminishing to very low levels within the wafers. No significant contaminants were found at the depth of the buffer/substrate interface. We also found no significant differences between the FET wafers with acceptable buffer leakage and those with unacceptable buffer leakage.

There are many complexities and subtleties involved in AES, and the technique is regarded as a qualitative tool more than a quantitative tool. We plan to test the samples again with secondary ion mass spectroscopy (SIMS), a sensitive technique that should identify any contamination missed by the AES tests.

2.4.1.5 Experiment Four - Substrate Cleaning Tests

Although only the specially prepared Spectrum and the stock Airtron substrates showed improvement when subjected to the bake procedure, we reasoned that other methods of removing contamination, such as chemical or mechanical cleaning, might prove more useful. In experiment four, we evaluated the effects of various chemical and mechanical surface treatments on 29 substrate samples. The treatments we used consisted of the following:

1. Soak in NRS-250 alkaline solution, followed by scrubbing with a commercial wafer scrubber,

2. Degrease in hot trichlorethane, acetone, and methanol, followed by a light etch in 1:1:8:NH_4OH:H_2O_2 and then scrub using deionized water,

3. A light etch only in the 1:1:8 solution followed by scrubbing,

4. No treatment, that is, use the substrates as supplied.

After treatment, we grew epitaxial test FET structures, fabricated ohmic contacts, etched the wafers leaving mesas, and tested the buffer resistance between pairs of mesas as in the earlier experiments.

The results can be summarized as follows:

- The soak and scrub process (1) caused significant degradation of the buffer resistance in all cases
- Degreasing the substrates followed by etching (2) was no better than etching alone (3)
- Light etching (3) sometimes improved the buffer resistance by about two orders of magnitude, but reduced the buffer resistance by about 30 percent on wafers already exhibiting superior results
- The untreated substrates from the Hitachi yielded higher buffer resistance than the domestic suppliers in the tests.

Table 2-4 shows the mean buffer resistance using four vendor's substrates cleaned by the different methods. We measured the buffer resistance across four FET structures fabricated on each wafer sample, for a total of 29 x 4 = 116 measurements. The results in the table suggest that doing nothing ("None") produces the highest and most desirable buffer resistance, followed by etching/scrubbing.

TABLE 2-4. BUFFER LEAKAGE EXPERIMENT #4, MEAN BUFFER RESISTANCE (megohm/square) BY CLEANING METHOD.

Buffer Resistance By Cleaning Method					
Vendor (# Samples)	None	Soak/Scrub	Degrease/ Etch/Scrub	Etch/Scrub	Mean
Airtron (20)	75.	16.	111.	117.	86.
M/A-COM (4)	140	98	40	17.	71.
Spectrum (2)	61	--	--	170.	117.
Hitachi (3)	216.	--	--	--	216.
Mean:	123.	34.	99.	107.	100.

Table 2-5 shows the significance of the differences among the cleaning methods in terms of the probability that the mean buffer leakage from one cleaning method is actually the same as that for another cleaning method. Using the 5 percent level of significance as the cut-off, the soak/scrub technique significantly degrades the buffer leakage compared to all the other cleaning methods. Etching and scrubbing does not significantly degrade the buffer resistance compared to doing nothing.

TABLE 2-5. TESTS OF SIGNIFICANCE OF LEAKAGE RESULTS BETWEEN PAIRS OF CLEANING METHODS.

Student's t-test 2 Tailed Probability

	None	Degrease/ Etch/Scrub	Etch/Scrub	Soak/Scrub
None	--	0.908	0.633	0.001
Etch/Scrub	0.908	--	0.756	0.021
Degrease/Etch & Scrub	0.633	0.756	--	0.069
Soak/Scrub	0.001	0.021	0.069	--

Comparing the buffer resistance results by vendor, we found that the Hitachi samples produced higher buffer resistance than the M/A-COM or Spectrum samples at the 2.0 percent and 1.7 percent levels of significance, respectively. Differences between other pairs of vendors were not significant at the 5 percent level.

We also measured breakdown voltage for the test FETs fabricated from the samples, as discussed in Monthly Progress Report 10, January 1990. The simple etch/scrub cleaning produced a slight improvement in breakdown voltage compared to doing nothing or subjecting the wafer to the more extensive cleaning methods, in agreement with the buffer resistance results. However, because of the large standard deviations in the voltage data for each vendor and cleaning method, the differences among the breakdown voltage results were not significant at the 5 percent level.

2.4.1.6 Additional Evidence Concerning Substrates

Upon completion of the substrate cleaning experiments, Spire scientists contacted Airtron, American Crystal Technology (AXT), Hitachi, M/A-COM, Semitronic, Showa-Denko, and Wacker to discuss our results and the availability of substrates suitable for epitaxial FETs.

According to the vendors, improper cleaning followed by storage of the substrates in plastic containers with unclean or uncured surfaces can cause contamination with hydrocarbons. Several vendors also showed us experimental evidence that the substrates favored by IC manufacturers, which have carbon background levels well below the 0.5 - 1E15 cm^{-3} range, produce good results for ion implanted FETs, but poor buffer leakage when used to fabricate epitaxial FETs. The optimum carbon background for epitaxial FETs is approximately 4 - 5E15 cm^{-3}, which corresponds to a substrate resistivity of greater than 5E7 ohm-centimeters.

These discussions convinced Spire of the importance of using "factory fresh" high resistivity substrates for the growth of FET wafers for delivery to the Phase I team. We decided to rely most heavily on material from Hitachi and Airtron, which provided the best buffer leakage results in our substrate experiments. We also decided to grow some of the FET wafers on substrates manufactured by American Crystal Technology and try Sumitomo "Improved Super Clean" wafers.

2.4.2 Optimization of Reactor Growth Conditions

Epitaxial growth experiments were performed using the modified reactor to determine the effects of susceptor temperature, reactor pressure, total gas flow rate, V/III ratio, trimethylgallium partial pressure, and dopant concentration. After optimizing the growth conditions based on these experiments, we reached ±3 percent in thickness uniformity and ±5 percent in doping uniformity over 80 percent of each wafer, exceeding the program goals. We also met the goal of attaining impurity concentrations below 1 x 10^{15} cm^{-3}.

Results of this work showed that the thickness uniformity was optimized at a reactor pressure of 50 torr and a total gas flow rate of 70 slpm. Typical undoped GaAs grown under these conditions has a background carrier concentration of 1.0 x 10^{14} cm^{-3} and 77 degree Kelvin mobility in excess of 70,000 cm $V^{-1}s^{-1}$. We evaluated both silane and disilane as dopant source gases for n-type material with disilane yielding superior uniformity at a growth temperature of 650°C.

2.4.2.1 Initial Reactor Growth Experiments

Prior to modification of the Model 1200 reactor for warm wall operation under the MIMIC program, we had attained a typical thickness uniformity of ±6 percent, and doping uniformity of ±12 percent, as shown in Table 2-6.

TABLE 2-6. UNIFORMITY GOALS FOR EPITAXIAL FET GROWTH.

	Attained Prior To MIMIC		MIMIC Goal*
	Best	Typical	
Thickness	±3%	±6%	±3%
Doping	±8%	±12%	±5%

*Over 80 percent of wafer.

During the initial growth tests at 60 slpm, we attained epitaxial layer thickness uniformity of ±5 percent, not adequate to meet the program goal. Wafers grown with flow rates of about 100 slpm exhibited thickness uniformities of better than ±3 percent, but with the thickest part of the growth shifted to the bottom of the wafers. This indicated insufficient depletion of the reactive chemical species in the boundary layer near the wafer surface, a condition which is remedied by reducing the flow rate. From these preliminary tests, we estimated the optimum flow rate for thickness uniformity to lie somewhere between 70 and 90 slpm at reactor pressures of 50 - 70 torr.

In subsequent growth experiments, we produced epitaxial layers with a thickness uniformity of ±2.2 percent on three-inch wafers. Experiments with adjacent two-inch wafers produced thickness uniformities of better than ±3 percent across four inches.

2.4.2.2 Wafer to Wafer Thickness Uniformity

We next mounted a full load of six wafers onto the susceptor, grew an epitaxial layer, and measured the thickness uniformity from wafer to wafer. As shown in Figure 2-6, the first test showed wide differences in the thickness (here expressed as growth rate) among the wafers. Because we rotate the susceptor during growth to minimize differences in growth conditions from wafer to wafer, this result surprised us, and we suspected a faulty susceptor.

To test the susceptor, we numbered the susceptor's facets, each of which holds a wafer during growth. We discovered that the epitaxial layer thickness depended on the facet. Careful measurement showed that the susceptor was not centered on its rotating support rod (Figure 2-7). Once we adjusted the position of the susceptor on the rod, the wafer to wafer thickness uniformity improved dramatically, as shown in Figure 2-8. The six wafers in this run have a top to bottom thickness uniformity of ±2.5 percent, with a wafer to wafer thickness uniformity of ±2.5 percent.

For MESFET production we will make minor modifications to the reaction chamber, for example the addition of base plate positioning screws, all designed to make positioning of the susceptor and support rod easier in a production environment.

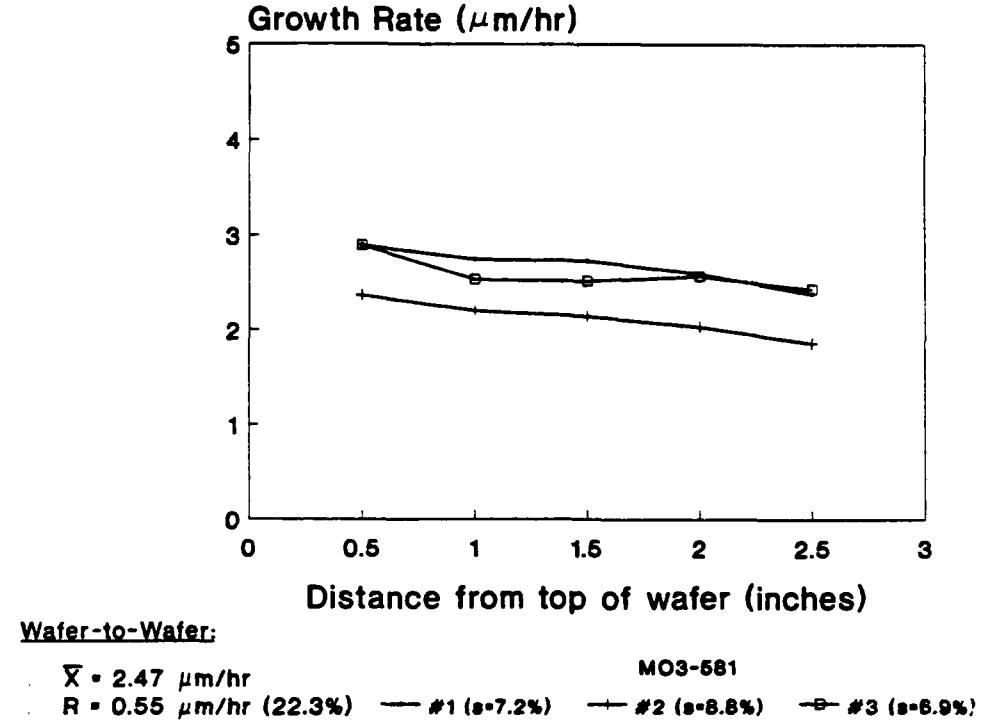


FIGURE 2-6. INITIAL GROWTH RATE UNIFORMITY (THREE WAFERS).

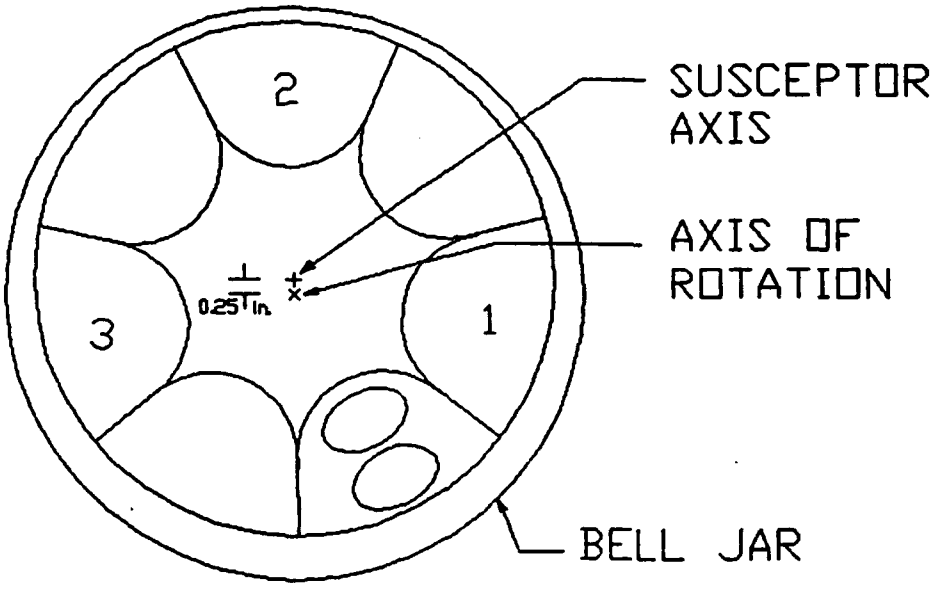


FIGURE 2-7. OBSERVED SUSCEPTOR CENTERING ERROR.

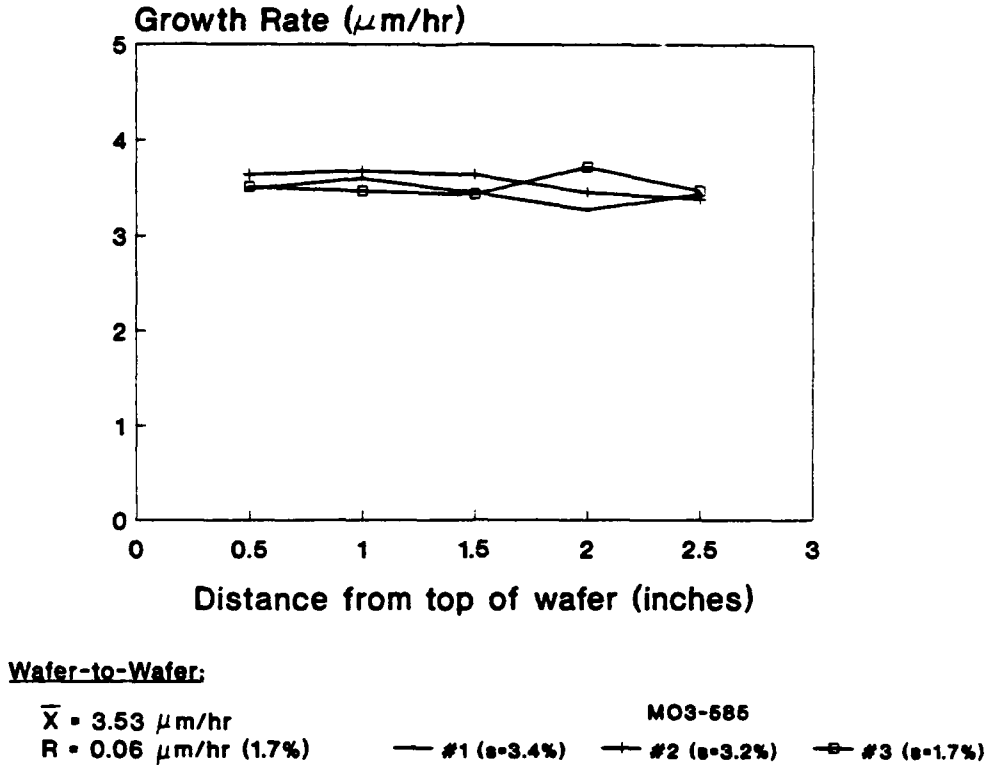


FIGURE 2-8. IMPROVED GROWTH RATE UNIFORMITY (THREE WAFERS).

2.4.2.3 Doping Uniformity

During separate growth experiments, silane or disilane were added to the reactant gases to produce silicon doped (n-type) epitaxial layers. The chemical dissociation of disilane gas into silicon is less temperature dependent than the dissociation of silane, and therefore disilane should lead to more uniform wafer doping.

In the first doping experiments, we attained a doping uniformity of approximately ±10 percent across each wafer using silane. Experiments confirmed the superiority of disilane in the new reactor when, after just a few runs, we attained doping uniformities of better than ±5 percent. The experiments were carried out using carrier concentrations in the range of 0.5×10^{18} to $1.0 \times 10^{18} cm^{-3}$. The measurements of carrier concentration (doping) are shown in Section 2.5.2 of this report.

2.4.2.4 Background Carrier Concentration and Mobility

Experiments to optimize the background carrier concentration and mobility of undoped gallium arsenide were begun as soon as the hydrogen booster pump and hydrogen purifier were installed. We initially adjusted the susceptor temperature indicated by the optical pyrometer to a value in the 500°C to 800°C range known to produce good material in Spire's smaller Model 450 MOCVD machines. The first wafers that we grew had a background carrier concentration

of approximately 6 x 10^{15} cm^{-3}, too high for good electrical characteristics. In subsequent tests we switched to higher purity source TMG and arsine, adjusted the V/III ratio, and progressively reduced the susceptor temperature. As a result we improved the background carrier concentration to the 7 x 10^{13} cm^{-3} range.

In a subsequent experiment we deposited an evaporated aluminum film on the susceptor and then slowly raised the susceptor temperature. At the melting point of the aluminum, 660°C, the optical pyrometer indicated a temperature of approximately 560°C. This gave us a valuable temperature calibration point for later experiments.

Gallium arsenide exhibits high electrical mobility only if it is highly pure. To improve the electrical mobility of our gallium arsenide layers, first we carefully cleaned the reactor system. The introduction of hydrogen chloride (HCl) vapor to perform an in situ etch of the bell jar and susceptor proved problematic because of the chlorides of arsenic and gallium generated in the process. Removing this toxic "black goo" required the complete disassembly and tedious scrubbing of the reactor chamber. The HCl also attacked the "O-ring" seals used in the chamber.

To overcome the difficulty of cleaning the system, we developed a wet etch technique whereby the susceptor and bell jar are removed and cleaned using an acid solution. This requires the use of a silicon carbide coated susceptor to prevent absorption of the acid solution by the susceptor. Desorption of the acids during epitaxial growth will interfere with the purity and mobility of the epitaxial layers.

With additional work to locate and seal small gas system leaks, clean the reactor, and optimize the V/III ratio, we obtained 77 degree Kelvin mobility in excess of 70,000 cm $V^{-1}s^{-1}$. The mobility data are discussed and shown in Section 2.5.4.

2.4.2.5 Buffer Quality

In April of 1990, Spire attained material with very high resistivity, which we believed would allow the fabrication of FETs with no buffer leakage. Therefore, we began to grow FET structure wafers with highly resistive buffer layers for delivery and evaluation by Raytheon and Texas Instruments. The first of these FET wafers exhibited an apparent carrier concentration peak in the buffer region which Spire, Texas Instruments, and Raytheon engineers believed would cause buffer leakage. After numerous experiments, we concluded that additional work beyond the scope of the contract would be required for the complete understanding and control of buffer quality.

The structure for the first FET wafers that Spire grew for delivery was as follows:

Substrates:	Semi-insulating, 75 mm diameter
Layer 1.	GaAs, undoped, 1.0 micrometer, buffer
Layer 2.	GaAs, N = 4E17, 0.2 micrometer, active

Spire had agreed to grow and deliver eight wafers with this structure to Raytheon and Texas Instruments for buffer leakage testing.

Spire grew the eight wafers for delivery and subjected a test sample to polaron testing. The sample exhibited a carrier concentration peak at the interface between the substrate and buffer layer as shown in Figure 2-9. According to Raytheon and Texas Instruments engineers, similar elevated carrier concentration readings have coincided with buffer leakage problems exhibited by finished FET devices.

Additional Polaron tests at Spire and Raytheon showed that all eight exhibited anomalous carrier concentration peaks in the buffer layers as described in Technical Report Number 13. Spire scientists proposed four different explanations to account for the buffer layer problem:

1. Surface or bulk contamination of the "as received" substrates.

2. Contamination of the buffer layer originating in the reactor, possibly from silicon vaporized from the hot bell jar wall.

3. Surface conditions during growth of the interface between the buffer and the substrate. These conditions may lead to charge carriers that cause buffer leakage. For example, surface decomposition, which creates arsenic vacancies, could enhance carrier formation.

4. Limitations of the Polaron apparatus and measurement technique that might cause inaccurate carrier concentration readings for FET structure wafers.

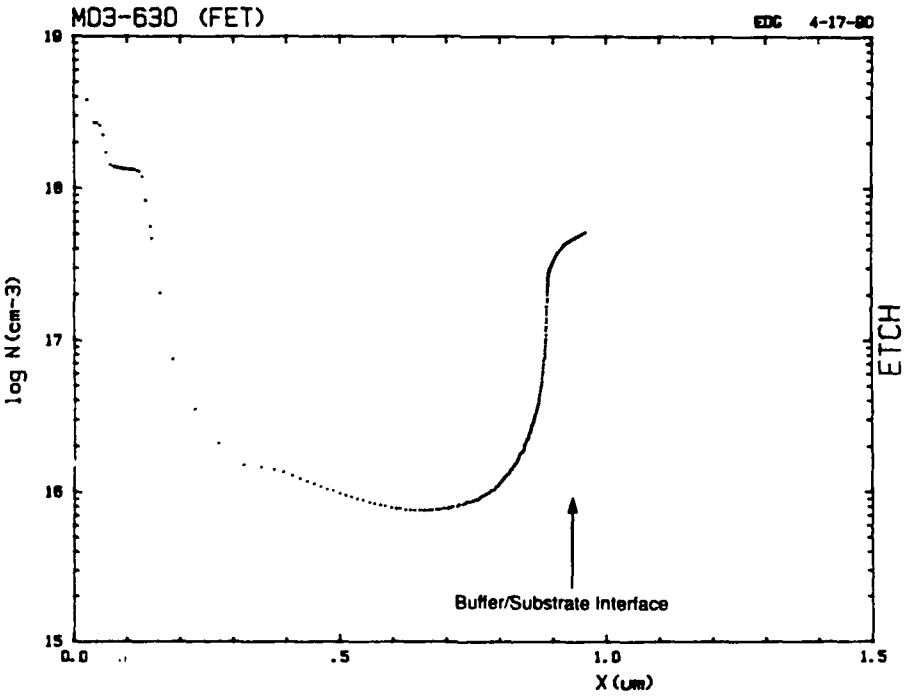


FIGURE 2-9. ANOMALOUS CARRIER CONCENTRATION AT THE BUFFER/SUBSTRATE INTERFACE.

Experimental tests of these explanations and the results are summarized below. Polaron plots for the various experiments are presented in Section 2.5.2.

Substrate Contamination - To test the hypothesis of contaminated substrates, we grew several wafers with the Raytheon FET structure on an assortment of substrate brands, including Hitachi, which usually produces devices with good buffer leakage according to our earlier substrate experiments. We also etched some of the substrates using the technique described in detail in the Section 2.4.1.5 of this report.

All of the wafers grown using the various substrates exhibited anomalous carrier concentrations in the buffer layer, although some of the AXT substrates showed less dramatic carrier concentration peaks.

Secondary ion mass spectroscopy (SIMS) and photoluminescence (PL) tests failed to reveal any contaminants in the buffer layers of test wafers that could account for the carrier concentration peak. Such contaminants cannot be completely ruled out because the SIMS and PL techniques are not sensitive enough to register very thin layers of contamination that could occur at the interface between the buffer and substrate. The SIMS and PL results are discussed in more detail in Section 2.5.5 of this report.

We concluded that substrate contamination may contribute to the carrier concentration peak, but it does not appear to be the sole cause of the problem.

Reactor Contamination - To test the hypothesis of reactor contamination, Spire grew the identical FET structure on 50 millimeter diameter wafers using a Model 450 reactor known to produce very high quality material for lasers, solar cells, HBTs, and other demanding structures.

All of the FET structure wafers grown on the Model 450 also exhibited the anomalous buffer peak. Therefore, we concluded that contamination in the new Model 1200 reactor was not the cause of the problem.

Initial Growth Conditions - To test the hypothesis that the initiation of growth plays a role, Spire scientists grew two buffer layers, one on top of the other. After growing the first buffer layer, the wafers were allowed to cool to room temperature. This terminated all growth and re-established the pre-growth ambient conditions. The wafers were then reheated and the second buffer layer grown. If the anomalous peak were to remain in the first buffer layer, this would imply a substrate related problem. If the peak were to move to the second layer, or if a peak were to appear in each buffer layer, this would imply a problem related to growth start-up.

After growing wafers with the double buffer layer structure, polaron plots confirmed that the doping hump had moved into the second (top) buffer layer. This implies that conditions during the initiation of growth lead to epitaxial material that exhibits the buffer leakage problem.

In another experiment, Spire grew a thin AlGaAs layer on the substrate before growing the FET structure. Because the bandgap of the AlGaAs should isolate the FET from the

substrate, we reasoned that the AlGaAs layer would eliminated the anomalous carrier concentration peak if this were caused by carriers at the interface between the substrate and the buffer. Polaron measurements showed that the AlGaAs layer had indeed eliminated the carrier concentration peak.

In subsequent experiments, Spire scientists grew a series of FET wafers, altering the V/III ratio and wafer temperature for each during the initiation of buffer growth. We then examined the carrier concentration profiles in the buffer layers of the wafers by polaron, as before. We reasoned that the initial growth conditions should affect the crystalline quality of the interface and play a role in the removal of any native defects in the substrate such as arsenic vacancies or anti-site defects. These experiments showed that starting the wafer growth with arsenic-rich conditions reduced the height of the anomalous carrier concentration peak in the buffer. However, we were unable to completely eliminate the peak.

Measurement Artifacts - Raytheon verified Spire's Polaron measurements showing th anomalous peak in all eight of the delivery wafers, but Raytheon used a Bio & Rad Polaro (C-V) apparatus nearly identical to that used by Spire. Practical considerations limit the accurac of the C-V technique, which can sometimes produce misleading results that could account f some or all of the anomalous peak.

The C-V technique uses a contact probe which forms a Schottky contact at the de depth into the wafer, and an Ohmic contact at the top of the wafer. The C-V method de on the relationship between applied voltage and measured capacitance for the determina carrier concentration. The C-V apparatus applies a small radio frequency signal betw probe and Ohmic contact and measures the capacitance by noting the phase shift in the r radio frequency current. This technique is applicable only if there no resistance bet probe point and contact.

As shown in Figure 2-10, the resistance between the Schottky contact and contact is a function of the depletion depth into the material. If the depletion depth the low doped buffer layer and semi-insulating substrate of the FET wafer, the r rise. This will decrease the measured capacitance, and in turn will produce an o the carrier concentration. Changes in area of the Schottky contact at depths a substrate could also contribute to capacitance and doping errors. See Reference discussion of C-V measurement errors.

Future Experiments - Additional work beyond the scope of the contra for the complete understanding and control of buffer quality. Spire will concentration of FET wafers by alternative methods such as step-wise C-V also fabricate FET test devices, measure buffer leakage, and check for cor doping profiles and actual buffer leakage on wafers grown with different i work will be completed after the termination of the contract, at Spire's

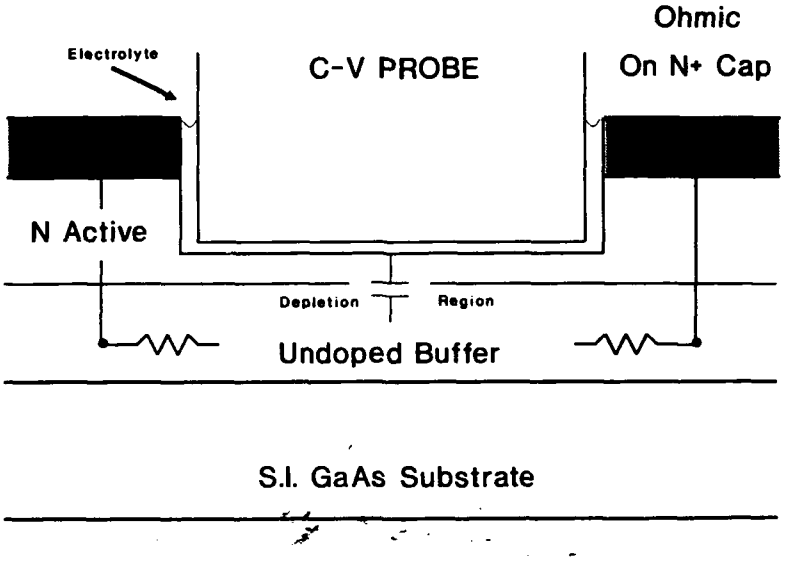


FIGURE 2-10. C-V MEASUREMENT OF FET WAFERS.

2.5 TASK 3.4 - CHARACTERIZE GROWN EPITAXIAL LAYERS

Characterization of the epitaxial layers grown on the new reactor is important for providing guidance for optimizing growth procedures. As discussed in the previous section, we measured parameters such as film thickness, carrier concentration and mobility, and adjusted the growth conditions for improved material.

2.5.1 Thickness

Spire measured the thickness of epilayers from numerous test wafers, finally attaining excellent thickness uniformity in a run of six wafers, as shown in Figure 2-11. Late in the year we delivered six wafers to Texas Instruments for thickness measurement. These wafers consisted of a single undoped GaAs layer, 0.3 micrometers thick, grown on n-type, 75 millimeter diameter substrates. Figure 2-12 shows thickness profiles for the six wafers, as determined by Texas Instruments. Approximately 85 percent of the 668 measurement points across the six wafers yielded thickness values within the ±3 percent target.

We also delivered six wafers consisting of an 0.3 micrometer $Al_{0.25}Ga_{0.75}As$ layer, capped with a 1,000Å layer of undoped GaAs, on N^+ substrates. Figure 2-13 shows thickness data for this lot of aluminum gallium arsenide (AlGaAs) wafers measured by Texas Instruments. The graph shows a systematic decrease in the AlGaAs thickness from the tops to the bottoms of the wafers. Further optimization in the growth conditions should lead to improved uniformity for AlGaAs layers, approaching the uniformities that we have attained with GaAs.

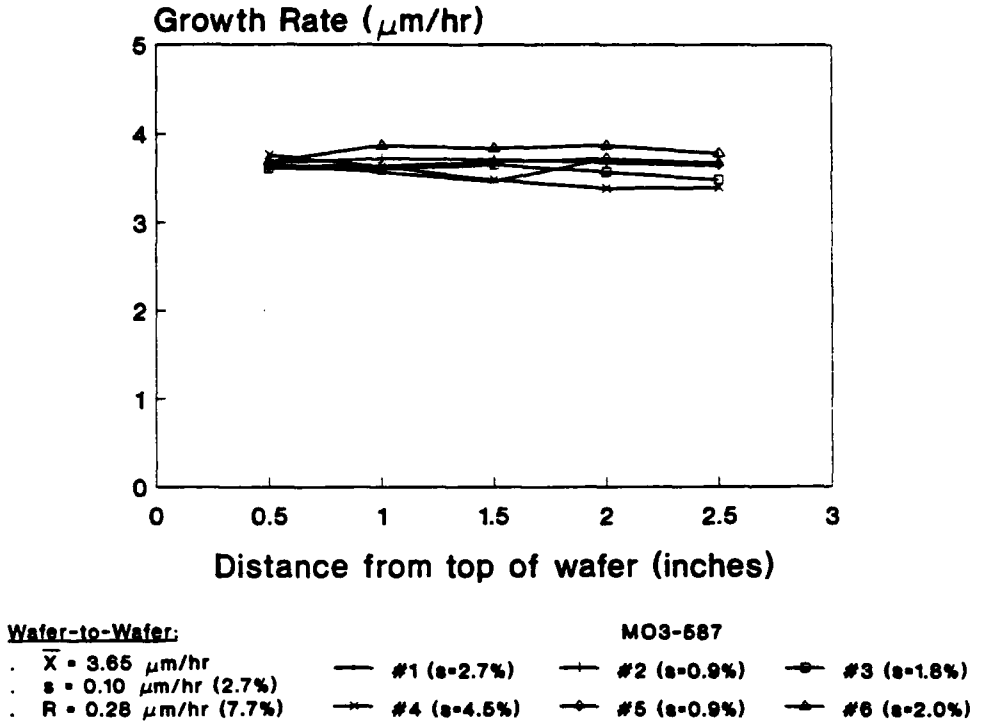


FIGURE 2-11. GaAs THICKNESS/GROWTH RATE UNIFORMITY, FOR FULL LOAD OF SIX WAFERS MEASURED BY SPIRE.

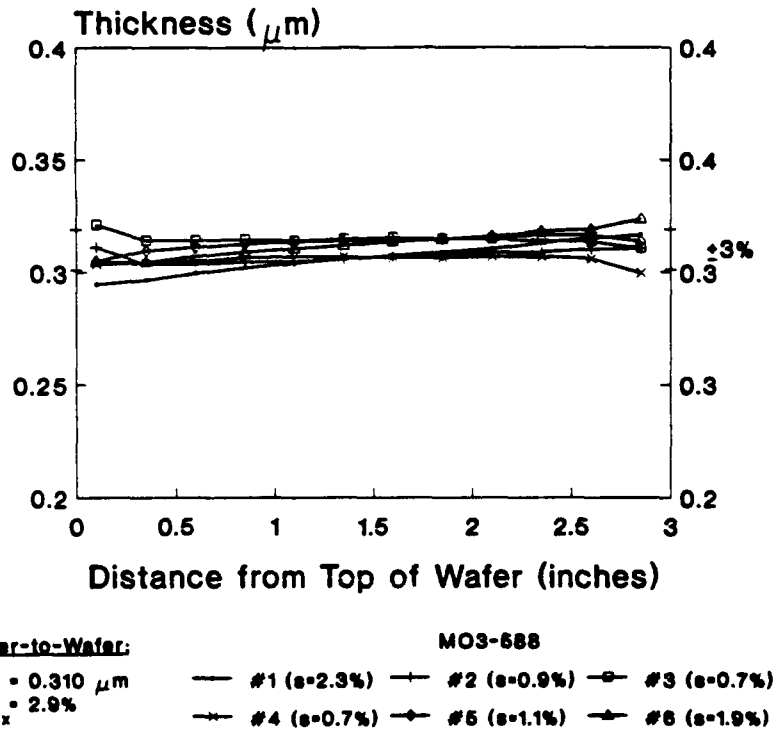


FIGURE 2-12. THICKNESS UNIFORMITY MEASURED BY TI.

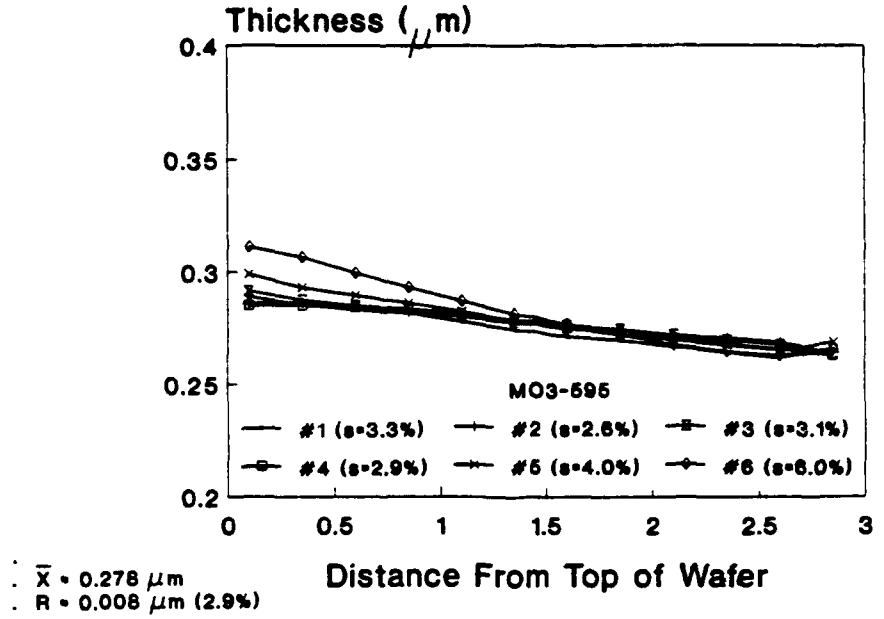


FIGURE 2-13. AlGaAs THICKNESS UNIFORMITY, MEASURED BY TI.

2.5.2 Doping

As explained in Section 2.4.2.3, Spire performed doping experiments using both silane and disilane as dopant source gases. Testing of the Polaron capacitance-voltage (C-V) profiler used for the measurements showed a measurement resolution as poor as ±10 percent in some ranges. After we made some software changes, the display resolution improved to approximately one percent.

Figure 2-14 shows a typical profile of the carrier concentration across a wafer resulting from n-type doping using silane. In the figure, the carrier concentration increases near the bottom of the wafer because of the dependence of cracking efficiency on temperature.

Figure 2-15 shows a typical carrier concentration profile across a wafer for two different layers doped with disilane. Because of the reduced dependence of the disilane cracking on temperature, the doping is much more uniform than that attained with silane.

We delivered six wafers to Texas Instruments for doping measurement. These wafers consisted of a single GaAs layer, 0.3 micrometers thick, doped to approximately $N = 5 \times 10^{17}$ cm^{-3}, grown on semi-insulating, 75 millimeter diameter substrates. Figure 2-16 shows the carrier concentrations measured at various locations on a 50 millimeter diameter test wafer from the run, as determined by Spire. The carrier concentrations are all the same within the experimental accuracy of the polaron profiler (about one percent). Figure 2-17 shows doping profiles for

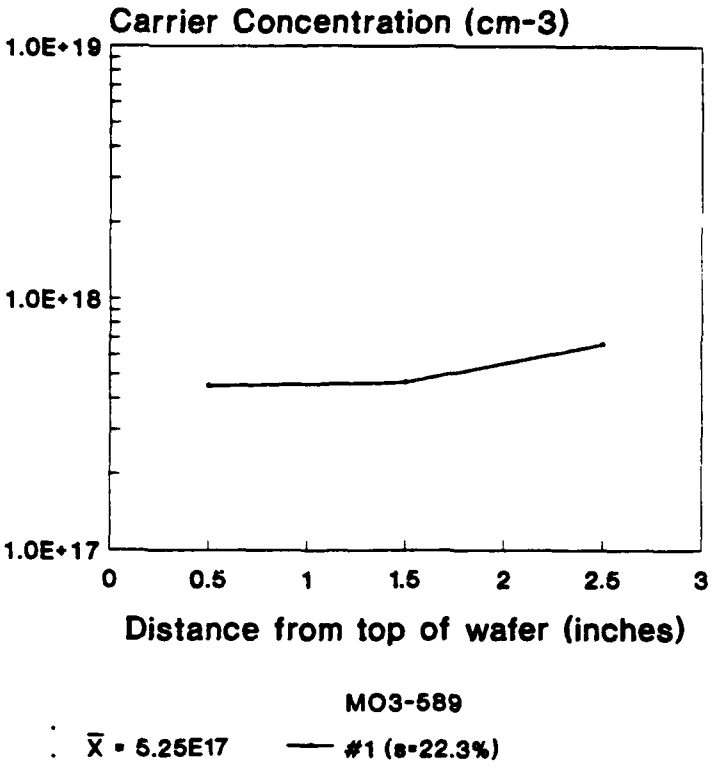


FIGURE 2-14. DOPING PROFILE - SILANE.

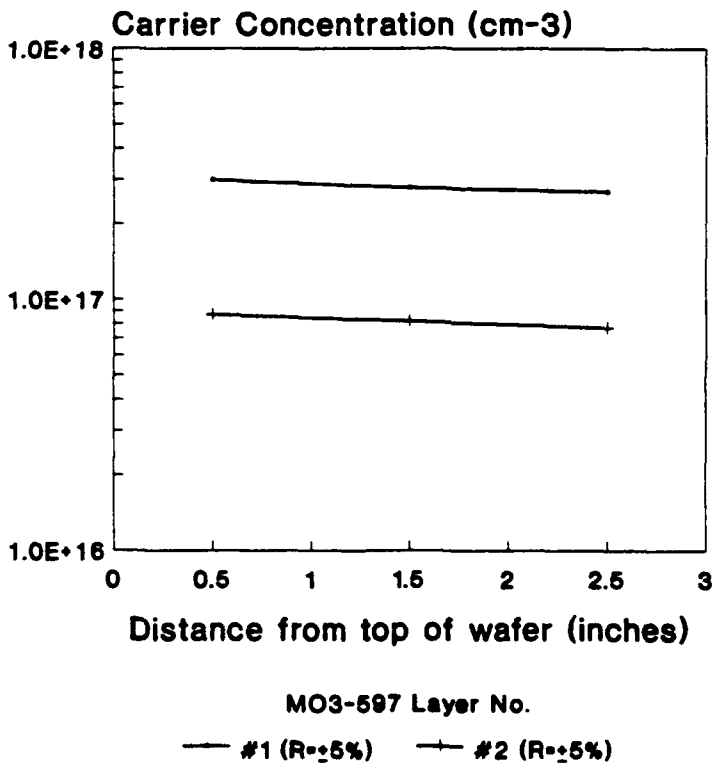


FIGURE 2-15. DOPING PROFILE - DISILANE.

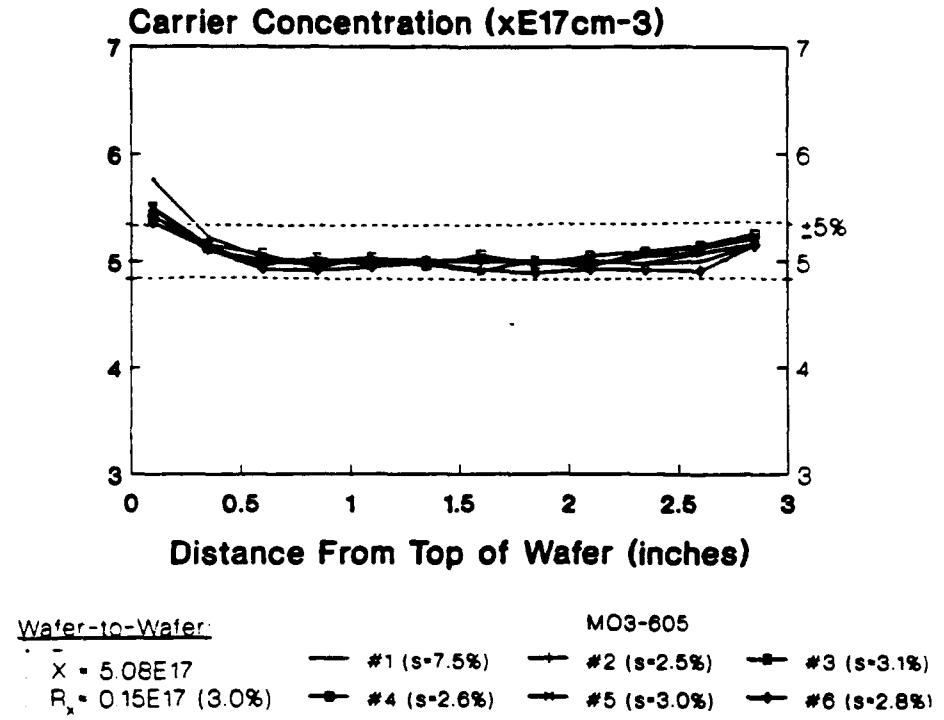


FIGURE 2-16. DOPING UNIFORMITY OF TI DELIVERY, MEASURED BY SPIRE ON TEST WAFER.

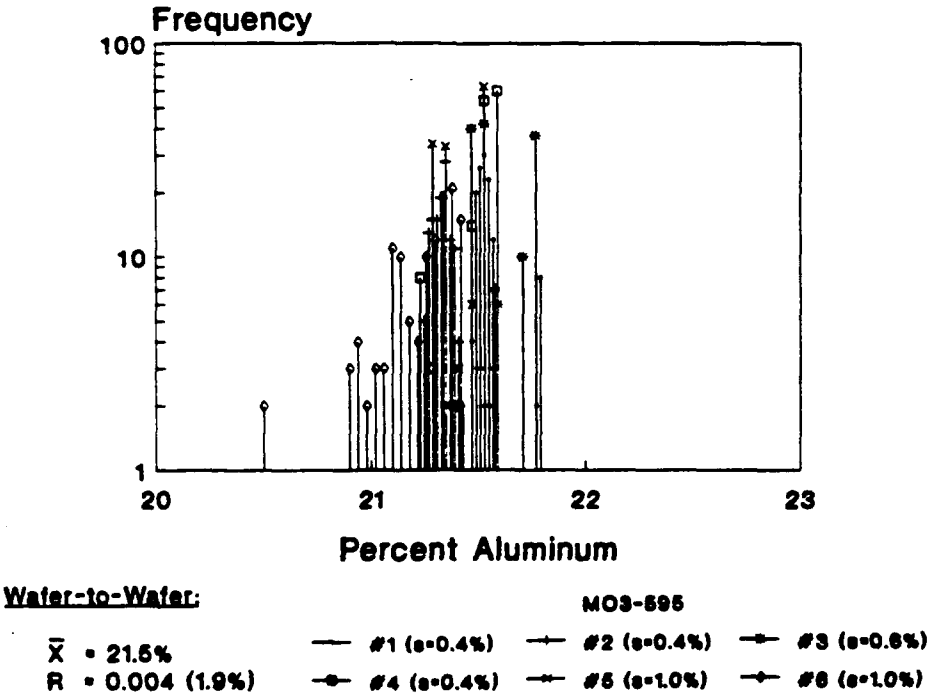


FIGURE 2-17. DOPING UNIFORMITY OF TI DELIVERY, MEASURED BY TI ACROSS SIX WAFERS.

the six wafers from the run, as determined by Texas Instruments. Approximately 82 percent of the 626 measurement points across the six wafers yielded doping values within the ±5 percent target. These wafers exhibited excellent surface morphology with fewer than 20 defects per square centimeter.

During the course of experiments to grow high quality buffer layers, Spire scientists performed numerous measurements of carrier concentration on FET structure wafers (see Section 2.4.2.6). Figure 2-18 shows a polaron plot for wafer M4-1532-2, an MOCVD FET structure wafer grown in one of Spire's commercial reactors under conditions known to produce

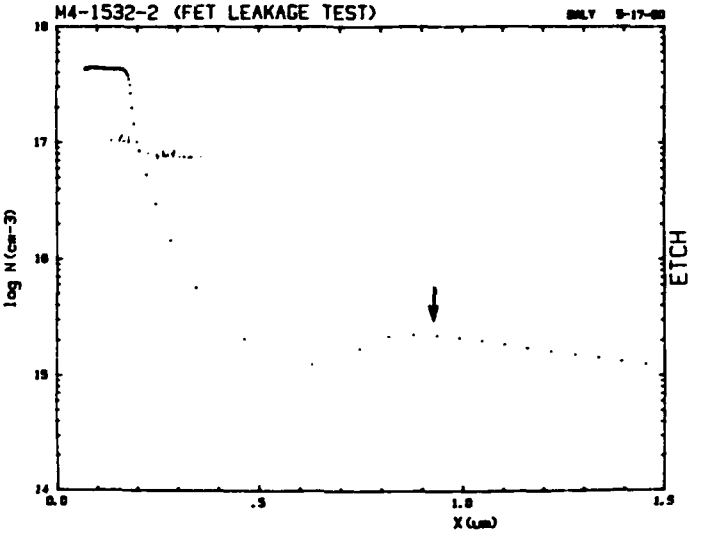


FIGURE 2-18. POLARON PLOT FOR RAYTHEON - TI FET STRUCTURE SHOWING ANOMALOUS BUFFER PEAK.

very high quality GaAs epitaxial layers. The wafer was grown to the same specifications requested by the Raytheon - Texas Instruments team for wafers intended for buffer leakage characterization. The polaron plot shows a carrier concentration peak with a value of about 2E15 cm^{-3} in the buffer layer in the vicinity of the buffer/substrate interface. It is generally believed that the exact location of the peak cannot be determined from the polaron plot because of capacitive effects during the measurement. For highly resistive buffer material, the carrier concentration should remain below 3E14. This wafer and the companion polaron plot were used as a "base case" for comparison purposes during subsequent experiments.

Figure 2-19 shows the polaron plot for a wafer grown with low arsine flow during the first seconds of growth. The arsine flow was slowly increased so that the V/III (arsenic to gallium) ratio started at 20 and then reached the approximately normal growth value of 67 after 30 seconds. The thickness of the first GaAs layer grown during this time was about 300 to 400Å. The polaron plot of Figure 2-19 indicates some improvement in the anomalous carrier concentration peak compared to the base case (Figure 2-18). Further decreases in the arsine flow would likely lead to decomposition of the GaAs substrate because of the high vapor pressure of arsenic.

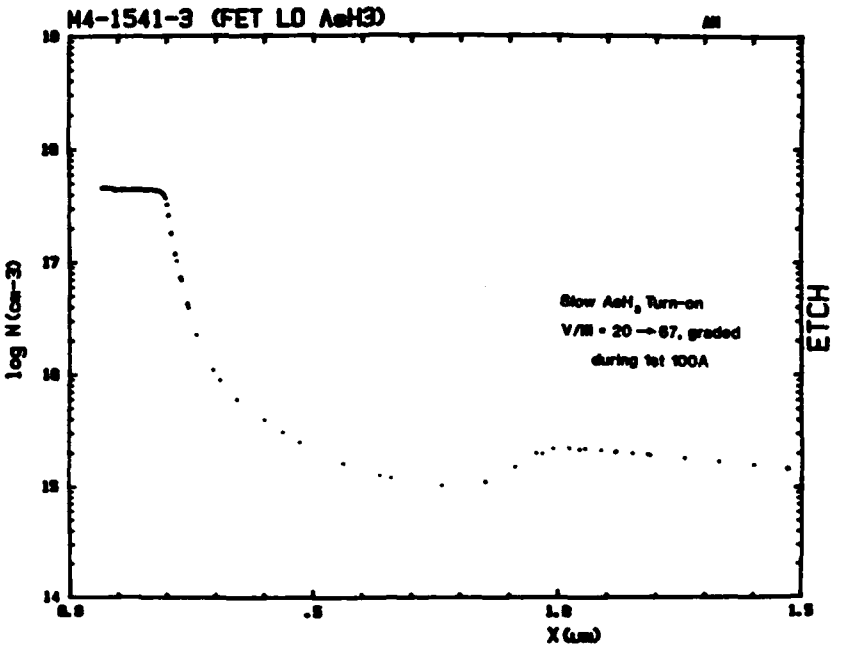


FIGURE 2-19. POLARON PLOTS FOR MOCVD FETs WITH VARIOUS INITIAL GROWTH CONDITIONS - LOW ARSINE FLOW.

Figure 2-20 shows the polaron plot for a wafer with a low temperature buffer. Instead of the usual 650°C wafer temperature, we grew the first 2,000Å of the buffer with a temperature of 500°C. We reasoned that the low temperature would result in a layer containing electrical traps that would enhance the insulating properties, therefore improving the buffer resistance. The polaron plot of Figure 2-20 shows no improvement in the anomalous carrier concentration peak compared to the base case. Without further tests we cannot determine how the low temperature conditions actually affected the crystalline quality or purity of the buffer.

Figure 2-21 shows the polaron plot for a wafer grown with low trimethylgallium (TMG) flow during the first seconds of growth. The flow was slowly increased so that the V/III ratio started at 450 and then fell to the approximately normal growth value of 70 after 30 seconds. The polaron plot indicates a worsening of the anomalous carrier concentration peak compared to the base case (Figure 2-18).

Figure 2-22 shows the polaron plot for a wafer with a low arsine and TMG flow during the initial 30 seconds of growth. Once again, the polaron plots shows the undesirable peak in the buffer.

Figure 2-23 shows the polaron plot for a FET test wafer with a two layer buffer. The initial layer on top of the substrate consists of 2,000Å of $Al_{0.3}Ga_{0.7}As$. The remaining 8,000Å of the buffer consist of the usual undoped GaAs. The polaron plot shows the desired carrier concentration profile for FETs, with no peak in the buffer. The large bandgap of the AlGaAs

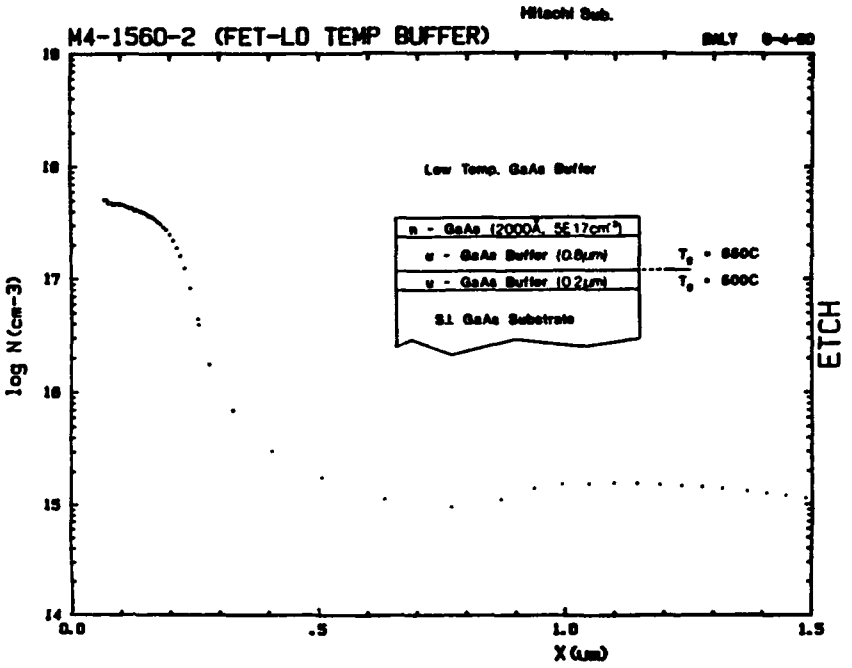


FIGURE 2-20. LOW TEMPERATURE BUFFER.

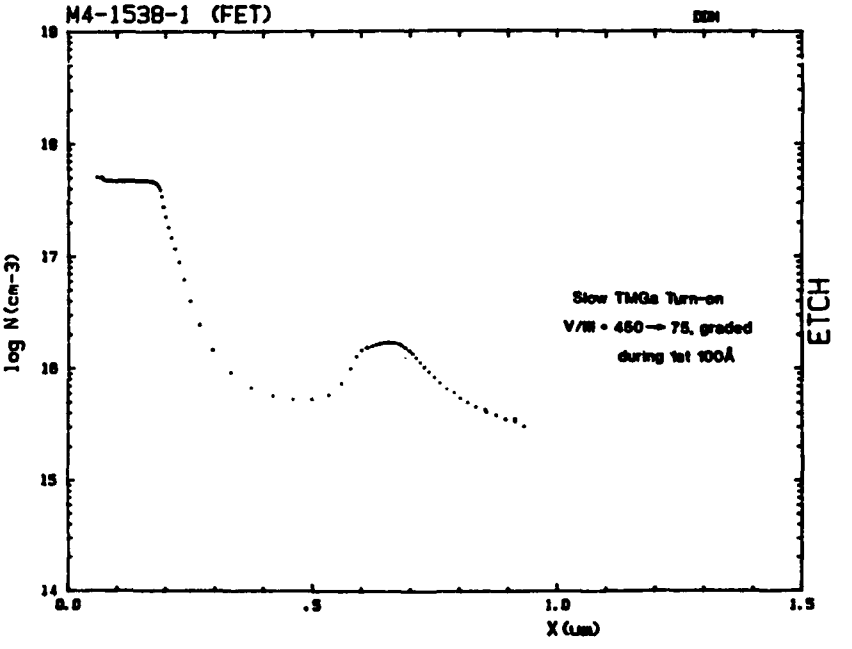


FIGURE 2-21. LOW TMG FLOW.

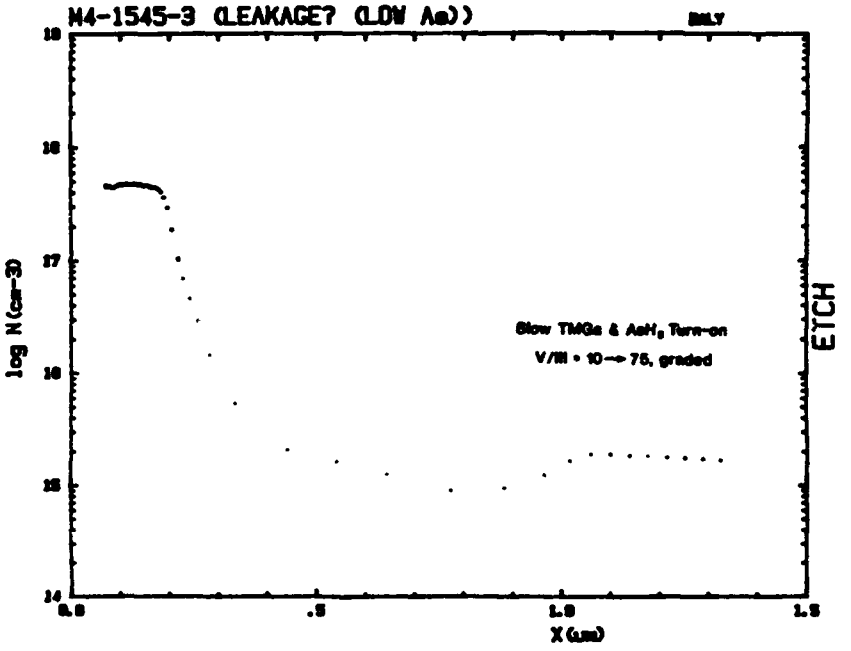


FIGURE 2-22. LOW TMG AND ARSINE FLOW.

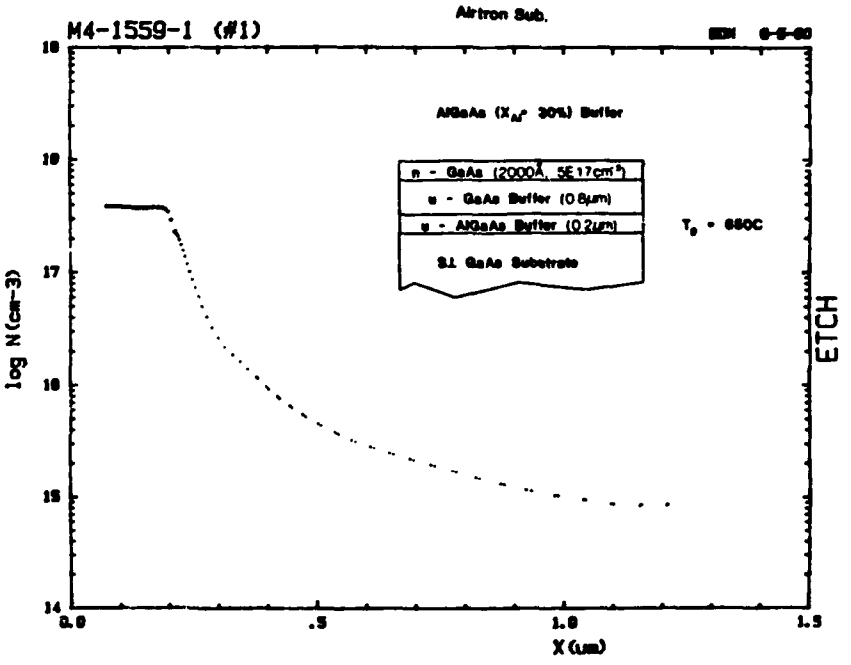


FIGURE 2-23. FET WITH AlGaAs BUFFER SHOWING NO BUFFER PEAK.

layer evidently acts as a barrier to any conduction through the substrate or the interface to the substrate. The plot supports the argument that buffer leakage is caused by the substrate interface. It can also be argued that the AlGaAs layer changes the depletion depth under the C-V measurement probe and reduces the series resistance, hence leading to more accurate polaron profiles.

Substrate Tests - To test the effects of substrate surface contamination, Spire cleaned several substrates with chemical etching solutions, and then sent them to Texas Instruments for MBE growth of the same structure as the base case wafer. We reasoned that because MBE produces high quality FET wafers, any significant substrate contamination would show up as differences in the polaron plots for differently treated substrates. Although substrate cleaning showed promise earlier in the program for reducing MOCVD FET buffer leakage, more recent results had not shown any differences in the anomalous carrier concentration peak when starting with different substrates.

We subjected one wafer to a 1/1/8 solution of $NH_4OH:H_2O_2:H_2O$, a light etchant that will improve the buffer resistance of substrates with contaminated surfaces, as demonstrated earlier in the program. Another wafer was subjected to a 5/1/1 solution of $H_2SO_4:H_2O_2:H_2O$, while another wafer was sent untreated.

Figures 2-24, 2-25, and 2-26 show the polaron plots for the MBE FET wafers grown on the three substrates. All show the same anomalous carrier concentration peak observed with MOCVD FET wafers. This result suggested to us that MBE wafers are susceptible to the same buffer quality problems as MOCVD or, alternatively, that the carrier concentration peaks are indeed measurement artifacts.

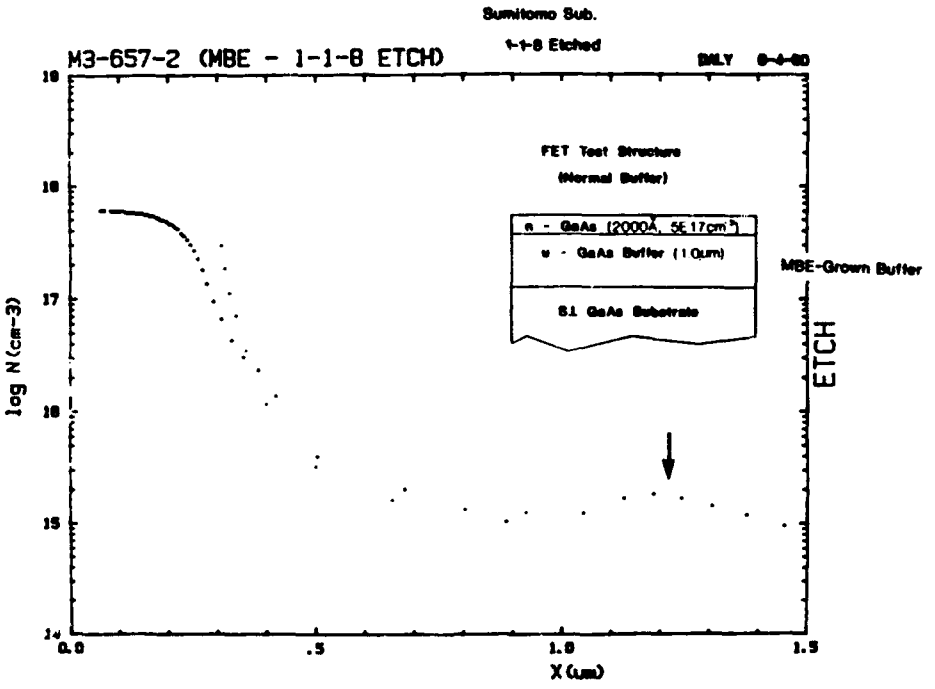


FIGURE 2-24. MBE FET, 1-1-8 ETCHED SUBSTRATE.

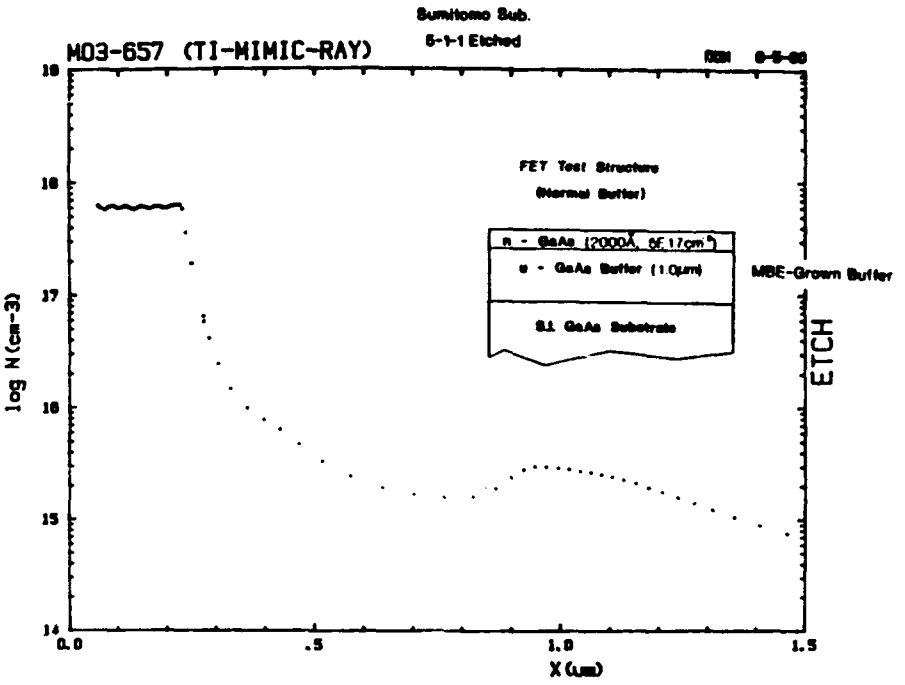


FIGURE 2-25. MBE FET, 5-1-1 ETCHED SUBSTRATE.

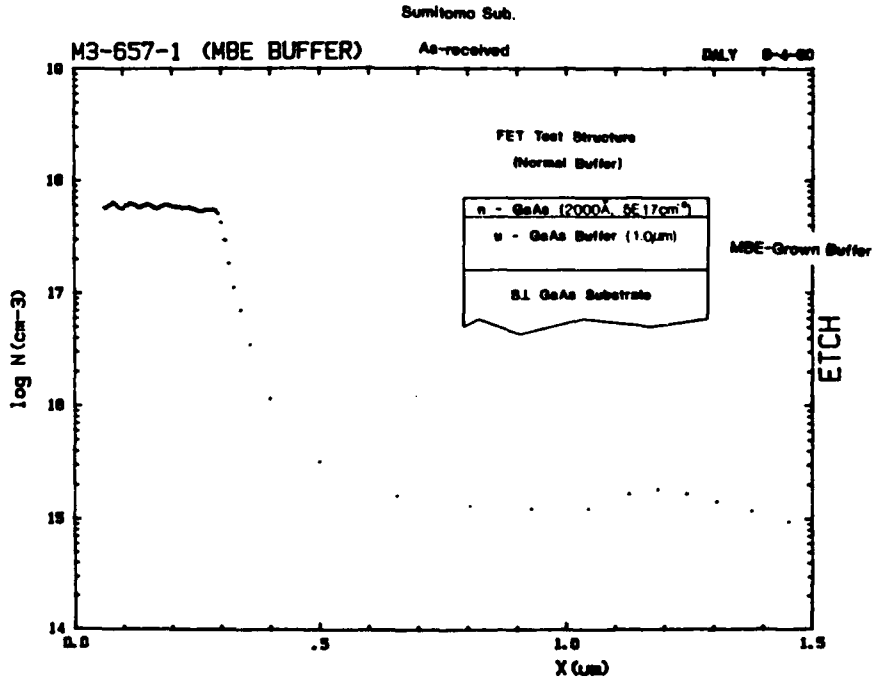


FIGURE 2-26. MBE FET, AS - RECEIVED SUBSTRATE.

2.5.3 Composition

Figure 2-27 shows the aluminum composition of AlGaAs layers on six undoped wafers delivered to Texas Instruments (See Section 2.5.1 and Figure 2-13). The mean layer composition across the six wafers was 21.5 percent, slightly off from the 25 percent target. This discrepancy is not serious and could have been reduced by more careful calibration and testing prior to the growth run. The compositional uniformity, defined as the standard deviation divided by the mean, ranged from 0.4 percent to 1.0 percent, while the wafer to wafer uniformity was 0.6 percent. Compositional epitaxial uniformity is important for advanced FET structures as well as HBTs and HEMTs. Texas Instruments researchers used scanning room temperature photoluminescence to measure the layer composition of these wafers.

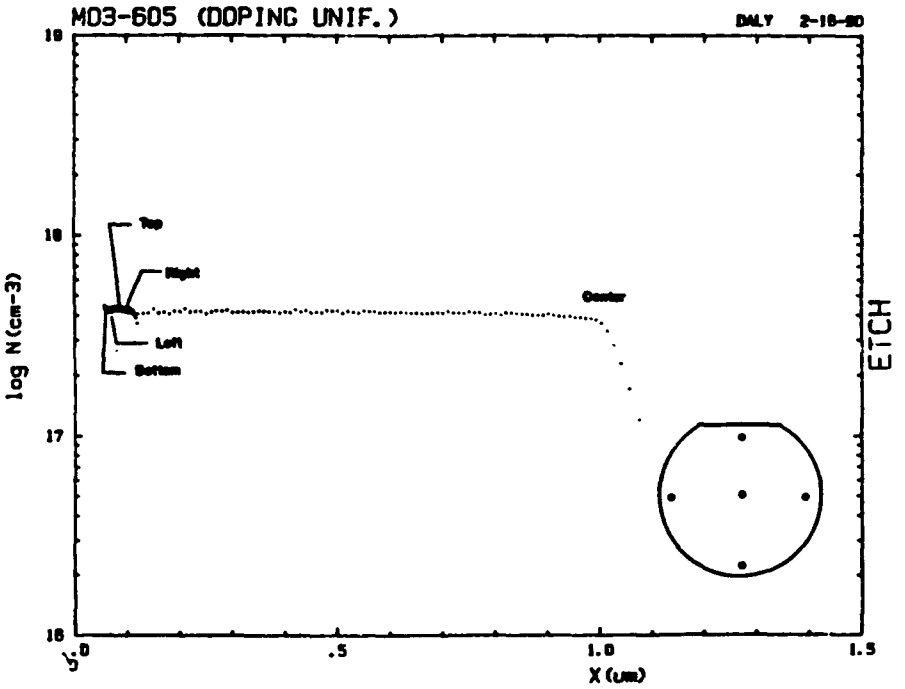
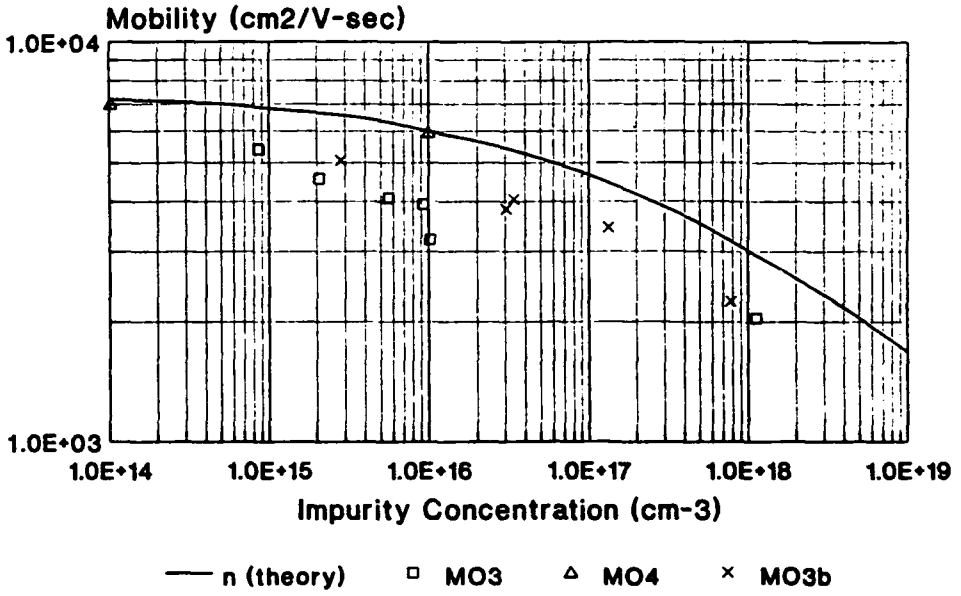


FIGURE 2-27. AlGaAs COMPOSITION, MEASURED BY TI.

2.5.4 Mobility

Figure 2-28 shows the electrical mobility of material from the modified reactor (MO3 and MO3b) as determined by Hall measurements. From the most recent measurement we obtained room temperature mobilities corresponding to a 77°K mobility in excess of 70,000 cm $V^{-1}s^{-1}$. With more work to reduce background contamination and optimize the growth conditions, we expect to attain mobility values similar to those attained in our Model 450 reactor, which are very close to the theoretical limits.



After S.M. Sze, Physics of Semiconductor Devices (New York:Wiley) 1969.

FIGURE 2-28. MOBILITY MEASUREMENTS SHOWING MO3 AND MO3B FROM NEW REACTOR.

2.5.5 Photoluminescence and Secondary Ion Mass Spectrometry

Dr. Gus Witt of the Massachusetts Institute of Technology, who has been funded by DARPA to correlate material properties to device performance, volunteered to test several samples of Spire's FET material. He concluded that impurities attached to a GaAs vacancy/interstitial complex at the interface between the buffer and the substrate could explain the anomalous buffer layer doping profiles.

Dr. Witt based his conclusions primarily on data from photoluminescence (PL) and secondary ion mass spectrometry (SIMS) measurements on three Spire epi wafers. The wafers tested were three of the same wafers subjected to Polaron measurement by Spire, as discussed in the June 1990 MIMIC Monthly Report and in the previous sections of this report:

1. M4-1538: Slow TMGa initiation with a V/III ratio changing from 450 to the approximately normal 75 during the first 100Å of growth (see Figure 2-21);

2. M4-1559: FET test wafer with a 0.2 micrometer thick AlGaAs layer (see Figure 2-23). This wafer showed no anomalous carrier concentration peak;

3. M4-1560: Low temperature buffer layer, grown at 500°C (see Figure 2-22).

Dr. Witt etched a staircase step pattern into each epi wafer using a (40:1:1) solution of H_2SO_4:H_2O_2:H_2O. He then obtained photoluminescence (PL) spectra from the surface of each step and compared the spectra as a function of depth.

Figure 2-29 shows the PL spectrum at the top surface of wafer M4-1538. The spectrum shows two sharp peaks corresponding to transition energies of 1.51 eV and 1.49 eV, and a broad spectrum which can be resolved into two peaks, one at 1.463 eV and the other at 1.431 eV. The 1.51 eV peak corresponds to the bandgap of gallium arsenide, while the other peaks correspond to donor-acceptor impurity transitions. Spectra obtained at depths of 1,000Å and 2,000Å, still well above the 12,000Å deep buffer/substrate interface, show little change from Figure 2-29.

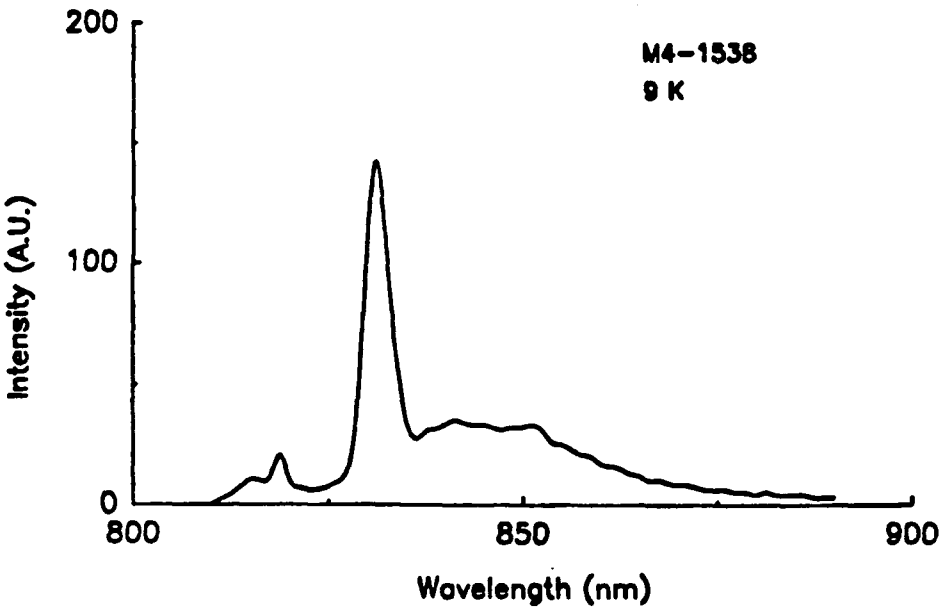


FIGURE 2-29. PL SPECTRUM OF THE TOP SURFACE OF WAFER M4-1538 (SLOW TMGa FLOW).

In sample M4-1559, the wafer with the AlGaAs buffer, the spectra show changes as a function of depth (Figures 2-30, 2-31 and 2-32). The spectrum taken at the top surface once again shows the peaks at 1.51 and 1.49 eV (Figure 2-30). In the spectrum taken after 1,000Å of surface removal (Figure 2-31), we see three additional peaks at 1.454, 1.359 and 1.324 eV. The 1.49 eV and 1.454 eV peaks increase in amplitude at a depth of 2,000Å, the depth of the top of the buffer layer. This could indicate a higher concentration of impurities in the buffer layer compared to the top (active) layer.

The spectra from sample M4-1560, the wafer with the low temperature buffer, show a similar trend (see Figures 2-33, 2-34, and 2-35). The 1.454 eV peak clearly increases in strength as a function of depth into the wafer, as does the broad low energy emission.

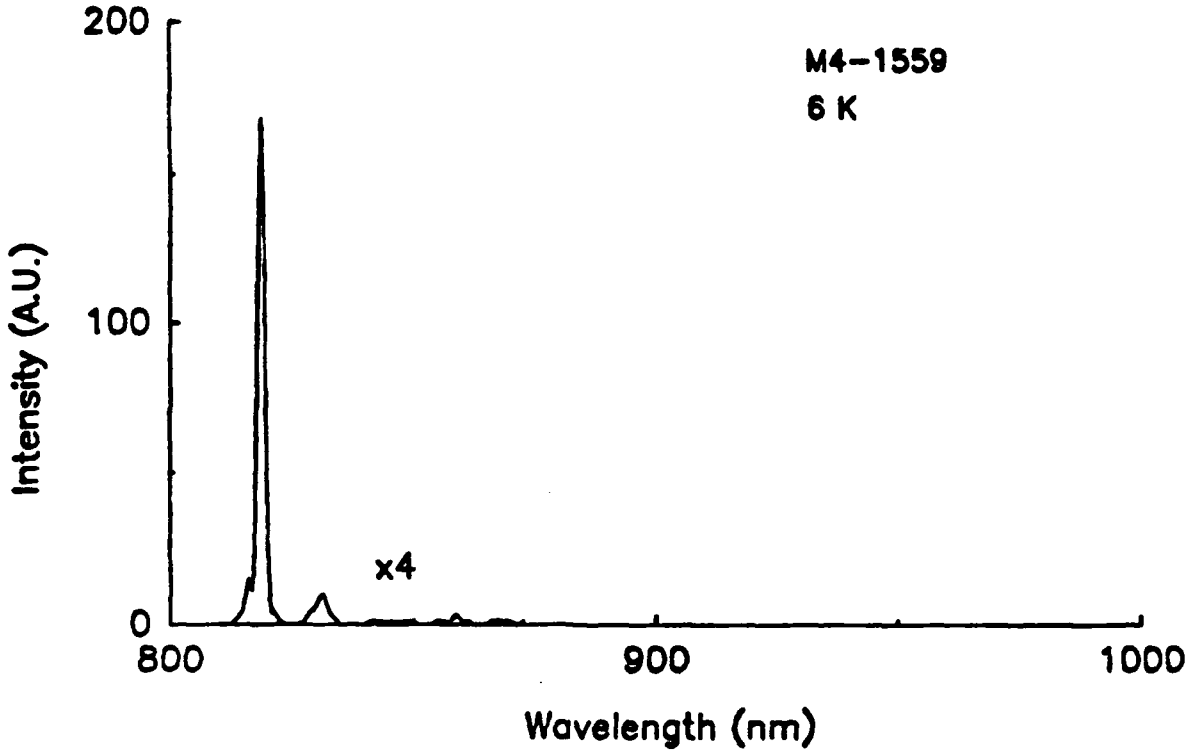


FIGURE 2-30. PL SPECTRUM OF TOP SURFACE OF SAMPLE M4-1559 (AlGaAs BUFFER).

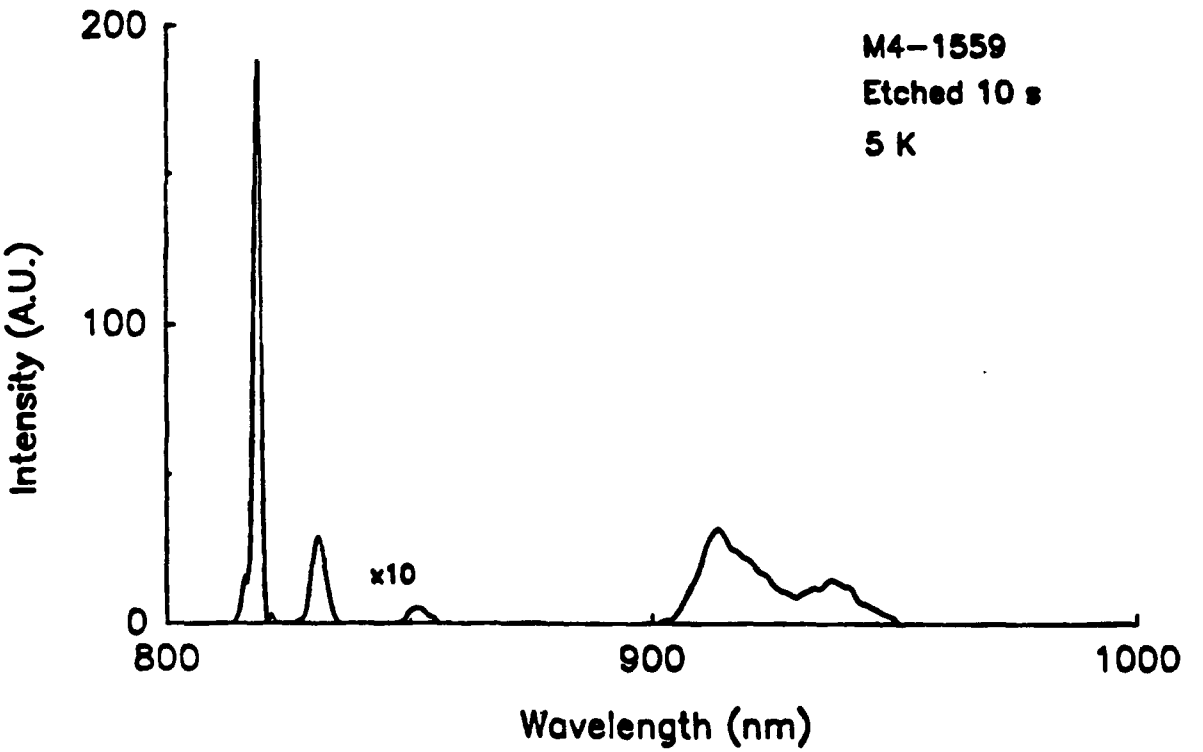


FIGURE 2-31. PL SPECTRUM OF M4-1559, AT A DEPTH OF 1,000Å.

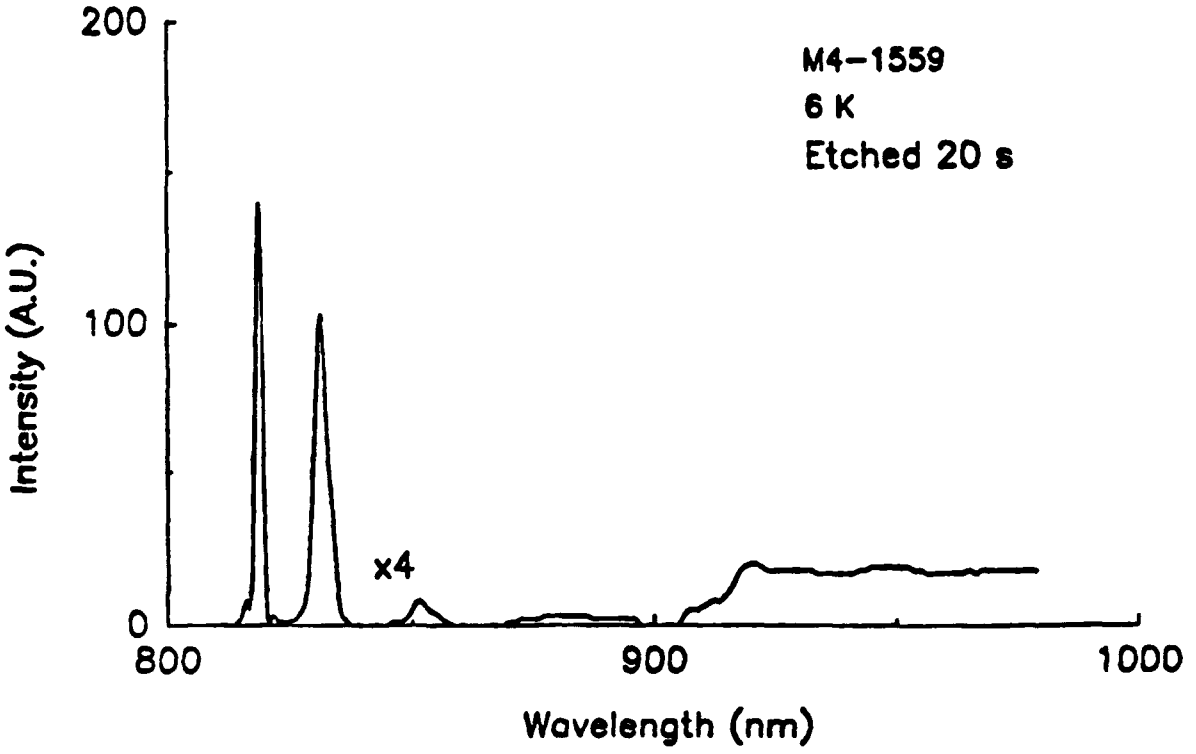


FIGURE 2-32. PL SPECTRUM OF M4-1559 AT A DEPTH OF 2,000Å.

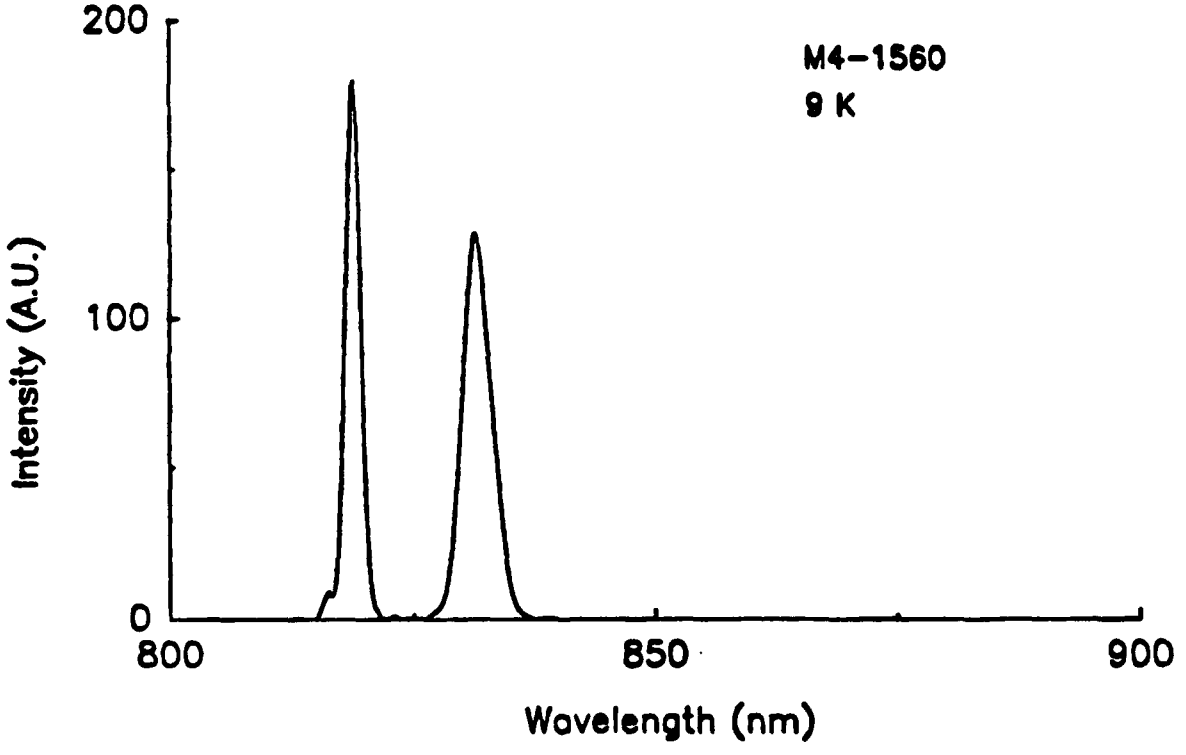


FIGURE 2-33. PL SPECTRUM OF TOP SURFACE OF M4-1560 (LOW TEMP. BUFFER).

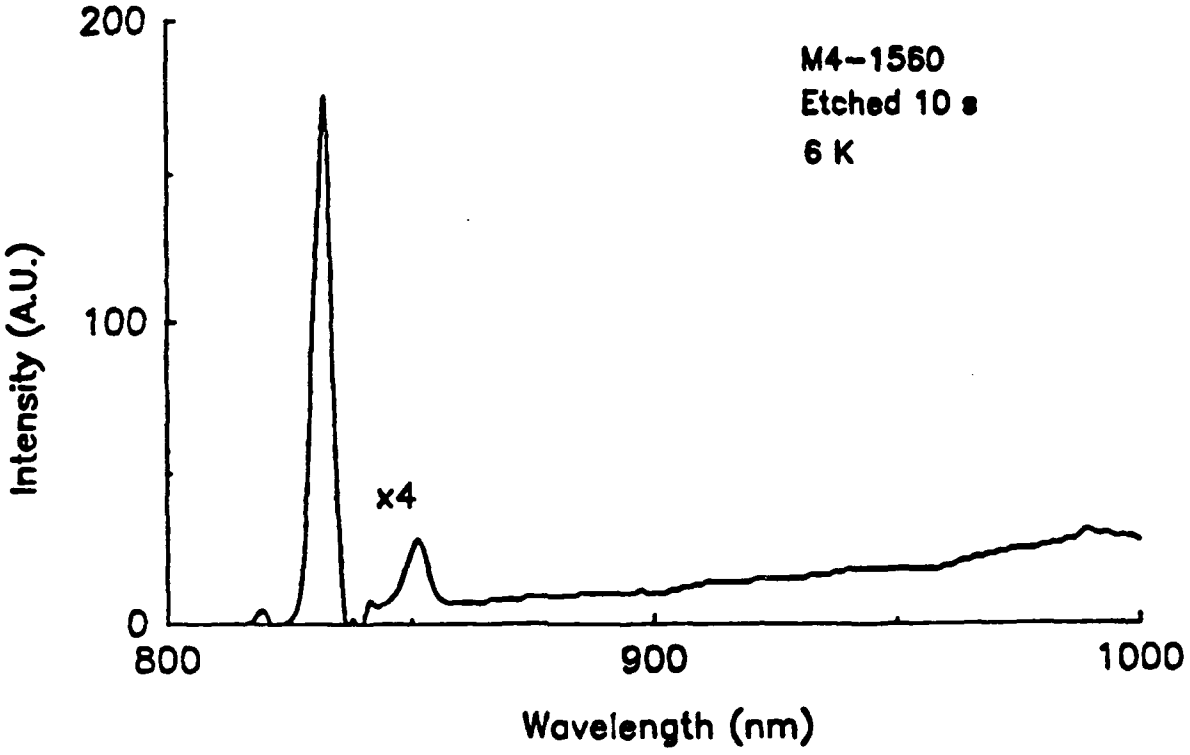


FIGURE 2-34. PL SPECTRUM OF M4-1560, AT A DEPTH OF 1,000Å.

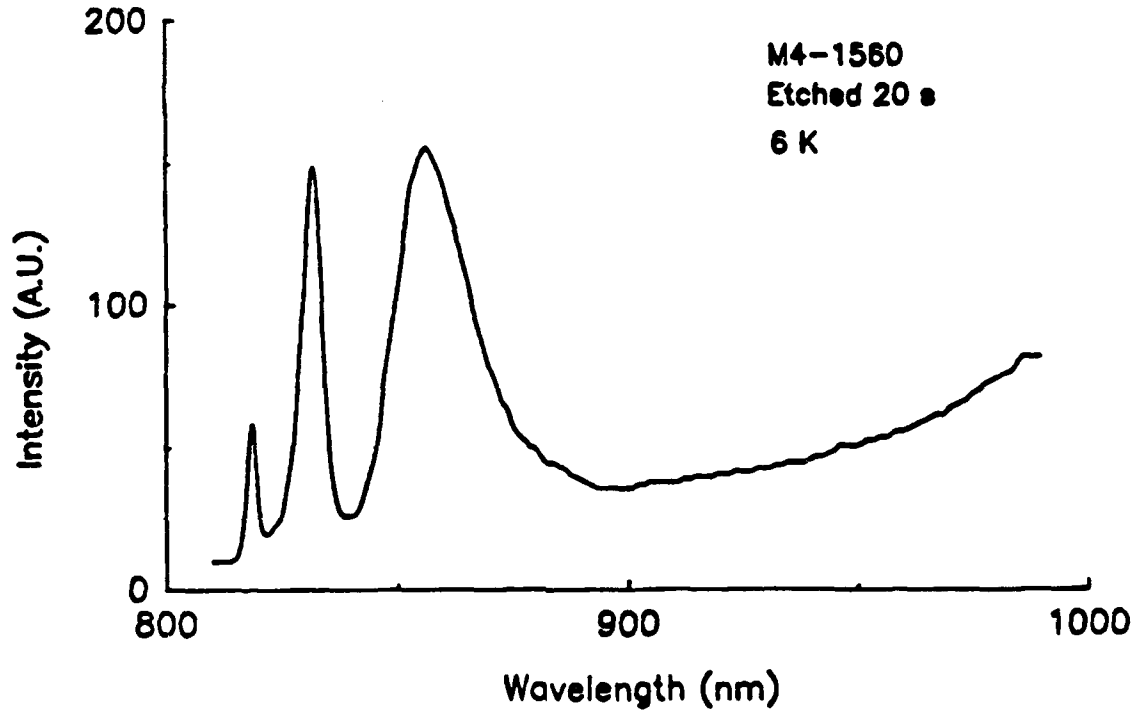


FIGURE 2-35. PL SPECTRUM OF M4-1560, AT A DEPTH OF 2,000Å.

Examination of the samples by SIMS revealed molecular oxygen (O_2) and carbon distributed evenly as a function of depth, but at very low levels. All three wafer samples looked approximately the same. The concentrations were so low that Dr. Witt could not rule out the possibility that the readings were caused entirely by trace impurities in the SIMS apparatus. Even though no significant impurities were discovered, a thin monolayer of electrically active impurities located at the buffer/substrate interface could cause buffer leakage and still escape detection by SIMS.

2.6 TASK 3.5 - INSERTION OF MOCVD WAFERS IN MIMIC PHASE I PRODUCTION

As explained in Section 2.8, an agreement was reached that Spire would deliver 50 wafers to the Raytheon/Texas Instruments team. Texas Instruments and Raytheon were willing to accept MOCVD wafers for production line insertion, but only after a qualification and testing phase that would reduce the possibility of costly production delays that could be caused by poor wafers.

The wafer delivery schedule was revised during the year to meet the objectives of the Navy, Texas Instruments, and Spire. As of June 1990, the list of deliveries was as shown in Table 2-7.

TABLE 2-7. WAFER DELIVERIES.

Delivery	Number, Type	Description/Structure	To
1.	Material Characteriz. 6 wafers Thickness Uniformity	N+ Substrates Layer 1: GaAs, undoped, 0.3 µm	TI
2.	Material Characteriz. 6 wafers Composition Uniformity	N+ Substrates Layer 1: 25% AlGaAs, undoped, 0.3 µm Layer 2: GaAs, undoped, 0.01 µm	TI
3.	Material Characteriz. 6 wafers Doping Uniformity	Si Substrates Layer 1: GaAs, N=5E17, 1.0 µm	TI
4.	Material Characteriz. 4 lots of 2 wafers Buffer layer quality	Si Substrates Layer 1: GaAs, undoped 1.0 µm Layer 2: GaAs, N=4E17 0.2 µm	TI and Raytheon 1/2 wafer each
5.	Device Test Number TBD Device Testing	Q-band FET Test Device	TI CR&D
6.	Process Monitor Number TBD	Q-band, Ka-band, and TBD	TI Raytheon
7.	Production insertion Number TBD	Various	TI Raytheon

Spire completed deliveries number 1, 2, and 3. Delivery number 4 consisted of eight wafers to be tested for thickness, doping, and buffer current leakage by Raytheon and Texas Instruments. Raytheon received the fourth delivery but returned the wafers to Spire without further work after noting the anomalous doping profile in the buffer region, as discussed in Section 2.4.2.5 of this report. Although Spire was unable to demonstrate that these wafers would make good FET devices before expiration of Spire's Phase 3 MIMIC contract, we will continue to work to develop a supply of high quality MOCVD grown FET wafers.

2.6 TASK 3.6 - DEVICE TESTING AND SCREENING OF EPITAXIAL WAFERS

The Raytheon - Texas Instruments team did not complete device testing and screening of epitaxial wafers because of the uncertainty about the quality of the buffer layers.

2.7 TASK 3.7 - COST ANALYSIS

The Statement of Work requires Spire to develop projections comparing the fabrication costs for MBE- and MOCVD-based MESFET circuits for MIMIC applications. The analysis consists of the elements shown in Figure 2-36 below:

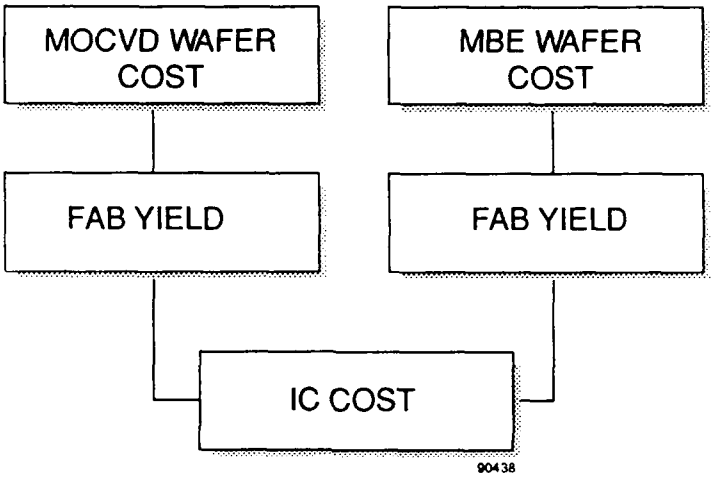


FIGURE 2-36. MIMIC IC COST ANALYSIS.

Texas Instruments and Raytheon did not process Spire MOCVD material into finished circuits in their chip production lines, so Spire does not have comparative fabrication yield information. However, based on our experience growing wafers under the MIMIC program for material characterization, we can make realistic projections of the cost of producing MOCVD MESFET wafers.

Figure 2-37 shows the results of our analysis of the costs per 75 millimeter MIMIC wafer produced by Spire's MOCVD. This is the cost of an MOCVD wafer before it is fabricated into ICs. For the analysis we assume MESFET wafers with a 1.0 micrometer buffer layer, an 0.25 micrometer active layer, and an 0.1 micrometer cap layer. The wafers that Spire delivered to Texas Instruments for material characterization cost us an estimated $4,819 each to produce. This cost is the result of the depreciation of capital equipment including equipment needed to modify the MOCVD apparatus, the many runs needed to establish optimum growth conditions, and scientific and engineering research support. The ratio of the number of wafers actually delivered to Texas Instruments to the number of times the machine has been run during this development phase is only about 0.6 wafers delivered per run. Note that the capacity of the machine was six wafers per run during Spire's MIMIC contract, but that during many early runs we limited the machine load to only one or two wafers per run to reduce substrate waste.

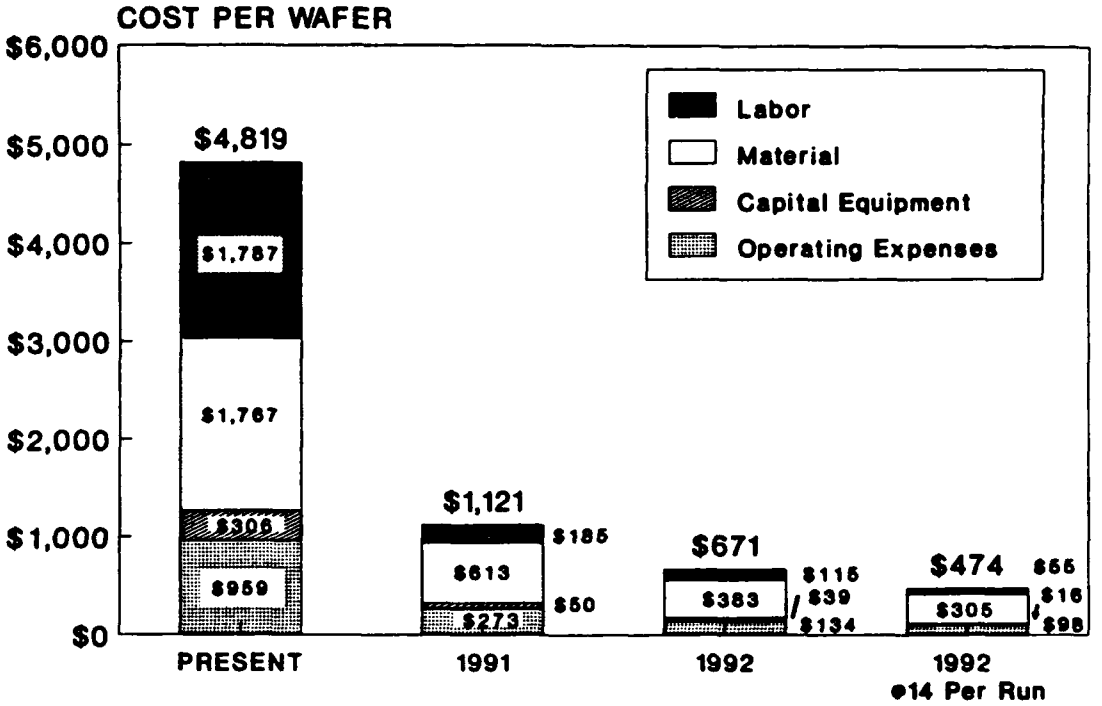


FIGURE 2-37. WAFER COST PROJECTIONS.

By 1991, we will have completed all of the process development work on the reactor. At this time, we will grow six MESFET wafers per run, except for the occasional calibration run of one or two wafers to verify machine set up. We expect production yields in the 60 to 70 percent range, and assuming deliveries of six to twelve wafers of a given structure, costs should fall below $1,122 per wafer.

With a seven wafer susceptor, a modest improvement in yields, and production of 28 or more consecutive wafers of the same structure to reduce the need for calibration runs, we expect production costs to fall below $671 per wafer. If we can use a susceptor capable of holding 14 wafers per run without serious impairment of the uniformity, production costs should fall below $474 per wafer.

2.8 REVIEWS AND DEBRIEFINGS

The original Statement of Work required Spire to supply Alpha Industries, a Phase I contractor, with wafers. In July 1989, Spire met with representatives of Alpha Industries to discuss the MIMIC program. Alpha Industries could not promise to process Spire's wafers without additional funding or a change in their own Phase I Statement of Work with the Army.

A few weeks later, Spire attended the Phase 3 MIMIC Kickoff Meeting at the Naval Research Laboratory. At this meeting, representatives of all four MIMIC Phase I teams expressed a strong interest in high quality, low cost MOCVD FET wafers. Spire explained the contractual difficulties with Alpha, and the Navy suggested that Spire might be able to supply

the Raytheon/Texas Instruments MIMIC Joint Venture team. Because the team's Phase I contract is also managed by the Navy, this would make coordination of the Spire Phase 3 and Phase I efforts more easily managed. Spire's Statement of Work was officially modified to substitute the Raytheon/Texas Instruments MIMIC Joint Venture for Alpha in August of 1989.

In November of 1989, Texas Instruments, Raytheon, and Spire representatives met and agreed upon a tentative wafer delivery schedule consisting of wafers for material characterization, device testing, fabrication line process monitoring, and finally production insertion. Work proceeded and Spire completed delivery of the first 18 wafers for material characterization.

In March of 1990, Spire presented a review of their MIMIC accomplishments at the Naval Research Laboratory including Dr. Gerry Borsuk, the COTR. Concern was expressed about the number and type of qualification wafers to be delivered to the Raytheon/Texas Instruments team, and a meeting was scheduled for the following month. At the April meeting, Spire, TI, Raytheon, and the Navy agreed to concentrate on demonstrating high quality buffer layers before proceeding with FET wafers for device test, fab line process monitoring, and insertion.

Spire also made presentations at the MIMIC Phase 3 Program Review, in March 1990, and the Annual MIMIC Conference in May.

SECTION 3
PROGRAM EXPENDITURES

Figure 3-1 shows cumulative program expenditures through to the termination of the program compared to planned expenditures. Unforeseen difficulties in modifying and making the reactor fully operational contributed to a faster than anticipated spending rate during the first year of the contract.

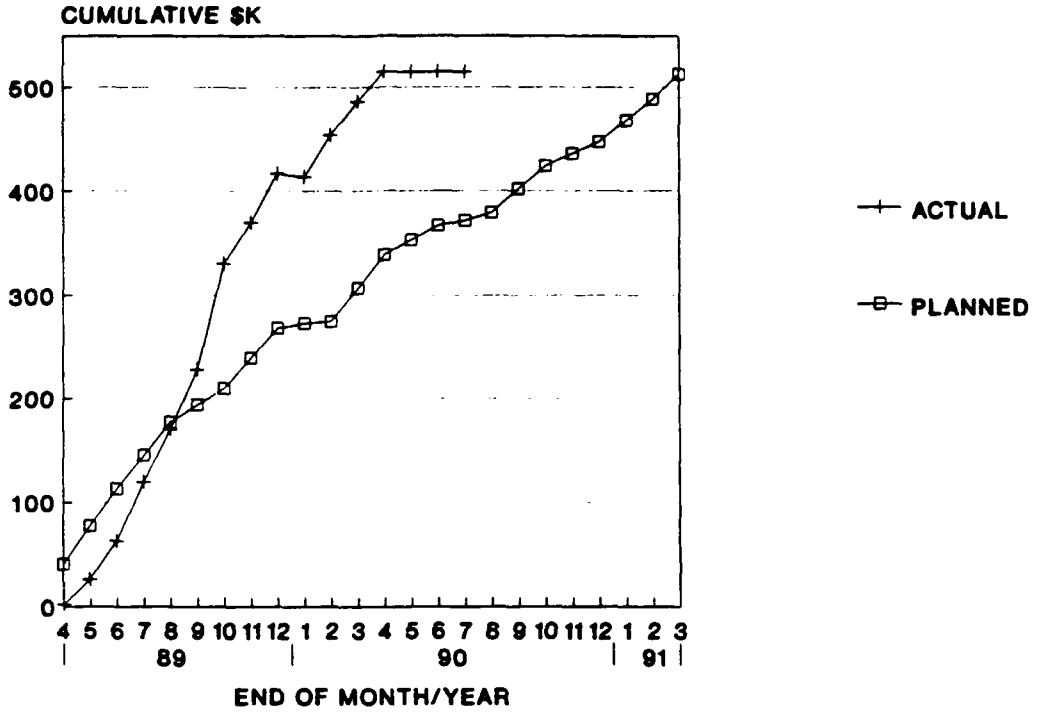


FIGURE 3-1. CUMULATIVE PROGRAM COSTS FOR JULY 1990.

Table 3-1 summarizes the cumulative contract expenditures in terms of direct labor, material, overhead, and general & administrative expenses. For details on the expenditures, the reader is urged to consult the Monthly Progress Reports, numbers one through sixteen.

TABLE 3-1. CONTRACT EXPENDITURES; APRIL 1989 - JULY 1990.

Expenditure	Labor	Overhead	Material	G & A	Total
Cumulative Total	$106,797.27	$190,009.55	$190,009.55	$109,482.50	$514,972.70

SECTION 4
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3. A. H. Dilawari and J. Szekely, J. Crystal Growth 97, 777-791 (1989).

4. Dieter K. Schroder, Semiconductor Material And Device Characterization, Wiley Interscience, New York, 1990, pp. 58 - 73.